



SPECIFICATION

SPEC. No. _____

DATE : Dec. 29. 2010

Customer

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME
MULTILAYER CERAMIC CHIP CAPACITORS
Array Series

Please sign and return this specification to your local TDK representatives. If orders are placed without this returned documentation, we must consider you found the specification acceptable.

THIS SPECIFICATION IS RECEIVED

DATE: _____ YEAR _____ MONTH _____ DAY _____

TDK-EPC Corporation
1-13-1, Nihonbashi, Chuo-ku, Tokyo
103-0027, Japan

ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office _____

Sales Tel. _____ () _____

PRODUCT CLASSIFICATION
CODE

040320

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd, TDK-EPC HONG KONG LIMITED, TDK (Malaysia) Sdn. Bhd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

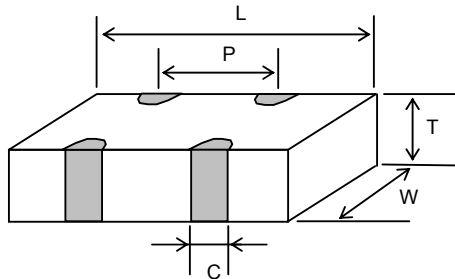
This specification warrants the quality of the TDK ceramic chip capacitors. The chips should be evaluated and confirmed in your product before use. If the use of the product exceeds the bounds of the specification, we can not guarantee its quality and/or reliability.

2. CODE CONSTRUCTION

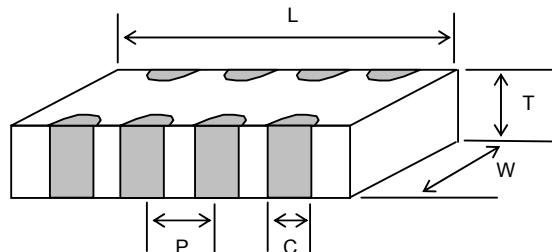
(Example)	<u>CKCM25</u>	<u>X7R</u>	<u>1H</u>	<u>102</u>	<u>M</u>	<u>T</u>
	<u>CKCL22</u>	<u>X5R</u>	<u>0J</u>	<u>105</u>	<u>M</u>	<u>T</u>
	<u>CKCL44</u>	<u>X7R</u>	<u>1E</u>	<u>103</u>	<u>M</u>	<u>T</u>
	<u>CKCA43</u>	<u>X7R</u>	<u>1H</u>	<u>102</u>	<u>M</u>	<u>T</u>
	(1)	(2)	(3)	(4)	(5)	(6)

1. Type

(2 element)



(4 element)



Please refer to product list for the dimension of each product.

2. Temperature Characteristics (Details are shown in Section No. 7 and No. 8.)

3. Rated Voltage

Symbol	Rated Voltage
2 A	DC 100 V
1 H	DC 50 V
1 E	DC 25 V
1 C	DC 16 V
1 A	DC 10 V
0 J	DC 6.3 V

4. Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and second digits identify the first and second significant figures of the capacitance; the third digit identifies the multiplier.

R is designated for a decimal point.

Example 102 → 1,000pF

105 → 1,000,000pF

5. Capacitance tolerance

Symbol	Tolerance	Capacitance
F	± 1 pF	10pF
K	± 10 %	Over 10pF
M	± 20 %	

6. Packaging

Symbol	Packaging
B	Bulk
T	Taping

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

1. Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance	Rated capacitance
1	C0G	F ($\pm 1\text{pF}$)	10pF
		K ($\pm 10\%$)	E – 6 series
2	X5R X7R	M ($\pm 20\%$)	E – 3 series

2. Capacitance Step in E series

E series	Capacitance Step					
E- 3	1.0		2.2		4.7	
E- 6	1.0	1.5	2.2	3.3	4.7	6.8

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X5R	-55°C	85°C	25°C
X7R C0G	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH
6 months Max.

6. INDUSTRIAL WASTE DISPOSAL

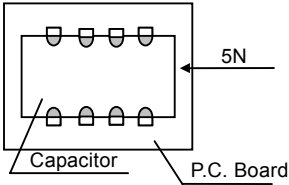
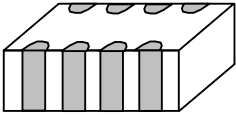
Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

7. PERFORMANCE

table 1

No.	Item	Performance	Test or inspection method									
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass (3X)									
2	Insulation Resistance	10,000MΩ min. (As for the capacitors of rated voltage 16, 10, 6.3V DC, 100MΩ·μF min.,) whichever smaller.	To measure between each terminal. Apply rated voltage for 60s.									
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	<table border="1"> <thead> <tr> <th>Class</th> <th>Apply voltage</th> </tr> </thead> <tbody> <tr> <td>Class 1</td> <td>3 × rated voltage</td> </tr> <tr> <td>Class 2</td> <td>2.5 × rated voltage</td> </tr> </tbody> </table> <p>Above DC voltage shall be applied across each terminal for 1 to 5s. Charge / discharge current shall not exceed 50mA.</p>	Class	Apply voltage	Class 1	3 × rated voltage	Class 2	2.5 × rated voltage			
Class	Apply voltage											
Class 1	3 × rated voltage											
Class 2	2.5 × rated voltage											
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Class</th> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>Class1</td> <td>1MHz±10%</td> <td>0.5-5Vrms.</td> </tr> <tr> <td>Class2</td> <td>1kHz±10%</td> <td>1.0±0.2Vrms.</td> </tr> </tbody> </table> <p>To measure between each terminal.</p>	Class	Measuring frequency	Measuring voltage	Class1	1MHz±10%	0.5-5Vrms.	Class2	1kHz±10%	1.0±0.2Vrms.
Class	Measuring frequency	Measuring voltage										
Class1	1MHz±10%	0.5-5Vrms.										
Class2	1kHz±10%	1.0±0.2Vrms.										
5	Q (Class 1)	<table border="1"> <thead> <tr> <th colspan="2">Specification</th> </tr> </thead> <tbody> <tr> <td>30pF and over</td> <td>Q ≥ 1,000</td> </tr> <tr> <td>Under 30pF</td> <td>Q ≥ 400+20·C</td> </tr> </tbody> </table> <p>C : Rated capacitance (pF)</p>	Specification		30pF and over	Q ≥ 1,000	Under 30pF	Q ≥ 400+20·C	See No.4 in this table for measuring condition.			
Specification												
30pF and over	Q ≥ 1,000											
Under 30pF	Q ≥ 400+20·C											
6	Dissipation Factor (Class 2)	<table border="1"> <thead> <tr> <th>Rated Voltage(V DC)</th> <th>D.F.</th> </tr> </thead> <tbody> <tr> <td>1E, 1H, 2A</td> <td>0.03 max.</td> </tr> <tr> <td>0J, 1A, 1C</td> <td>0.05 max.</td> </tr> </tbody> </table>	Rated Voltage(V DC)	D.F.	1E, 1H, 2A	0.03 max.	0J, 1A, 1C	0.05 max.	See No.4 in this table for measuring condition.			
Rated Voltage(V DC)	D.F.											
1E, 1H, 2A	0.03 max.											
0J, 1A, 1C	0.05 max.											
7	Temperature Characteristics of Capacitance (Class 1)	<table border="1"> <thead> <tr> <th>T.C.</th> <th>Temperature Coefficient</th> </tr> </thead> <tbody> <tr> <td>C0G</td> <td>0 ± 30 (ppm/°C)</td> </tr> </tbody> </table> <p>Capacitance drift within ± 0.2% or ± 0.05pF, whichever larger.</p>	T.C.	Temperature Coefficient	C0G	0 ± 30 (ppm/°C)	<p>Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature.</p> <p>Measuring temperature below 20°C shall be -10°C and -25°C.</p>					
T.C.	Temperature Coefficient											
C0G	0 ± 30 (ppm/°C)											

(7. Performance, continued)

No.	Item	Performance	Test or inspection method										
8	Temperature Characteristics of Capacitance (Class 2)	<p style="text-align: center;">Capacitance Change (%)</p> <hr/> <p style="text-align: center;">No voltage applied</p> <hr/> <p style="text-align: center;">X5R : ± 15</p> <p style="text-align: center;">X7R : ± 15</p> <hr/>	<p>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step. ΔC be calculated ref. STEP3 reading</p> <table border="1" data-bbox="987 359 1411 657"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>25 \pm 2</td> </tr> <tr> <td>2</td> <td>-55 \pm 3</td> </tr> <tr> <td>3</td> <td>25 \pm 2</td> </tr> <tr> <td>4</td> <td>Max. operating temp. \pm 2</td> </tr> </tbody> </table> <p>Measuring voltage: 0.1, 0.2, 0.5, 1.0Vrms. Product has which measuring voltage, please contact with our sales representative.</p>	Step	Temperature(°C)	1	25 \pm 2	2	-55 \pm 3	3	25 \pm 2	4	Max. operating temp. \pm 2
Step	Temperature(°C)												
1	25 \pm 2												
2	-55 \pm 3												
3	25 \pm 2												
4	Max. operating temp. \pm 2												
9	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) and apply a pushing force of 5N with 10\pm1s.</p> 										
10	Solderability	<p>New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of "A sections" shall not be exposed due to melting or shifting of termination material.</p>  <p style="text-align: center;">■ A section</p>	<p>Completely soak both terminations in solder at 235\pm5°C for 2\pm0.5s.</p> <p>Solder : H63A (JIS Z 3282)</p> <p>Flux : Isopropyl alcohol (JIS K 8839) Rosin(JIS K 5902) 25% solid solution.</p>										

(7. Performance, continued)

No.	Item		Performance	Test or inspection method															
11	Vibration	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) before testing. Vibrate the capacitor with amplitude of 1.5mm P-P changing the frequencies from 10Hz to 55Hz and back to 10Hz in about 1min. Repeat this for 2h each in 3 perpendicular directions.															
		Capacitance	Characteristics		Change from the value before test														
			Class 1		COG	$\pm 2.5\%$													
			Class 2		X5R X7R	$\pm 7.5\%$													
		Q (Class 1)	Rated Capacitance		Q														
30pF and over			1,000 min.																
Under 30pF			$400+20 \times C$ min.																
			C : Rated capacitance (pF)																
D.F. (Class 2)	Meet the initial spec.																		
12	Temperature cycle	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) before testing. Expose the capacitor in the conditions step1 through step 4 and repeat 5 times consecutively. Leave the capacitor in ambient conditions for 6 to 24h (Class 1) or 24 \pm 2h (Class 2) before measurement.															
		Capacitance	Characteristics		Change from the value before test														
			Class 1		COG	$\pm 2.5\%$													
			Class 2		X5R X7R	$\pm 25\%$													
		Q (Class 1)	Rated Capacitance		Q														
			30pF and over		1,000 min.														
			Under 30pF		$400+20 \times C$ min.														
					C : Rated capacitance (pF)														
D.F. (Class 2)	Meet the initial spec.																		
Insulation Resistance	Meet the initial spec.																		
Voltage proof	No insulation breakdown or other damage.																		
				<table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time (min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>-55 ± 3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>25 ± 2</td> <td>2 - 5</td> </tr> <tr> <td>3</td> <td>Max. operating temp. ± 2</td> <td>30 ± 2</td> </tr> <tr> <td>4</td> <td>25 ± 2</td> <td>2 - 5</td> </tr> </tbody> </table>	Step	Temperature(°C)	Time (min.)	1	-55 ± 3	30 ± 3	2	25 ± 2	2 - 5	3	Max. operating temp. ± 2	30 ± 2	4	25 ± 2	2 - 5
Step	Temperature(°C)	Time (min.)																	
1	-55 ± 3	30 ± 3																	
2	25 ± 2	2 - 5																	
3	Max. operating temp. ± 2	30 ± 2																	
4	25 ± 2	2 - 5																	

(7. Performance, continued)

No.	Item		Performance	Test or inspection method	
13	Moisture Resistance (Steady State)	External appearance	No mechanical damage.	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) before testing.</p> <p>Leave at temperature $40\pm 2^{\circ}\text{C}$, 90 to 95%RH for 500 +24,0h.</p> <p>Leave the capacitor in ambient conditions for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</p>	
		Capacitance	Characteristics		Change from the value before test
			Class 1		C0G
		Class 2	X5R X7R		$\pm 25\%$
		Q (Class 1)	Rated Capacitance		Q
	30pF and over	350 min.			
	10pF and over to under 30pF	$275+5/2\times C$ min.			
	Under 10pF	$200+10\times C$ min.			
			C : Rated capacitance (pF)		
D.F. (Class 2)	Characteristics X5R: 200% of initial spec. max. X7R: 200% of initial spec. max.				
Insulation Resistance	1,000M Ω min. (As for the capacitors of rated voltage 16, 10, 6.3V DC, 10M Ω · μF min.,)				
14	Moisture Resistance	External appearance	No mechanical damage.	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) before testing.</p> <p>Apply the rated voltage at temperature $40\pm 2^{\circ}\text{C}$ and 90 to 95%RH for 500 +24,0h.</p> <p>Charge/discharge current shall not exceed 50mA.</p> <p>Leave the capacitor in ambient conditions for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</p> <p>Voltage conditioning (only for class 2) Voltage treats the capacitor under testing temperature and voltage for 1 hour.</p> <p>Leave the capacitor in ambient conditions for 24±2h before measurement.</p> <p>Use this measurement for initial value.</p>	
		Capacitance	Characteristics		Change from the value before test
			Class 1		C0G
		Class 2	X5R X7R		$\pm 25\%$
		Q (Class 1)	Rated Capacitance		Q
	30pF and over	200 min.			
	Under 30pF	$100+10/3\times C$ min.			
			C : Rated capacitance (pF)		
D.F. (Class 2)	Characteristics X5R: 200% of initial spec. max. X7R: 200% of initial spec. max.				
Insulation Resistance	500M Ω or min. (As for the capacitors of rated voltage 16, 10, 6.3V DC, 5M Ω · μF min.,)				

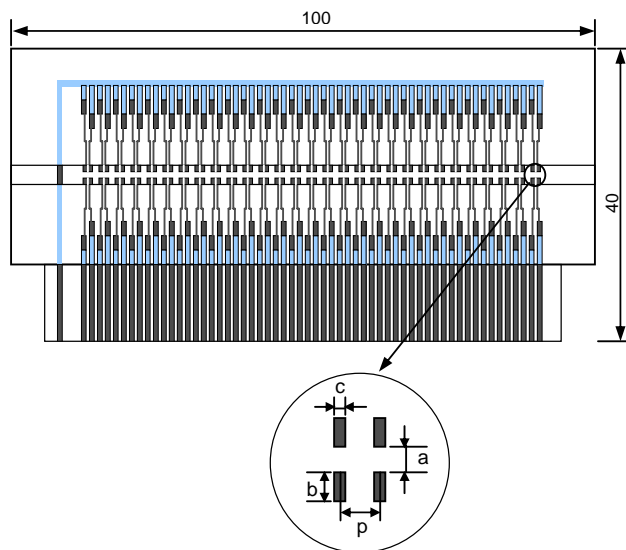
(7. Performance, continued)

No.	Item	Performance	Test or inspection method										
15	Life	External appearance	No mechanical damage.										
		Capacitance	<table border="1"> <thead> <tr> <th colspan="2">Characteristics</th> <th>Change from the value before test</th> </tr> </thead> <tbody> <tr> <td>Class 1</td> <td>C0 G</td> <td>± 3 %</td> </tr> <tr> <td>Class 2</td> <td>X5R X7R</td> <td>± 25 %</td> </tr> </tbody> </table>	Characteristics		Change from the value before test	Class 1	C0 G	± 3 %	Class 2	X5R X7R	± 25 %	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1 to 3) before testing.</p> <p>Below the voltage shall be applied at 125±2°C for 1,000 +48, 0h.</p> <p>Applied voltage is 1xRV. Some items may be tested at higher voltage (1.2x, 1.5x or 2xRV).</p>
			Characteristics		Change from the value before test								
			Class 1	C0 G	± 3 %								
		Class 2	X5R X7R	± 25 %									
Q (Class 1)	<table border="1"> <thead> <tr> <th>Rated Capacitance</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>30pF and over</td> <td>350 min.</td> </tr> <tr> <td>10pF and over to under 30pF</td> <td>275+5/2×C min.</td> </tr> <tr> <td>Under 10pF</td> <td>200+10×C min.</td> </tr> </tbody> </table> <p style="text-align: center;">C : Rated capacitance (pF)</p>	Rated Capacitance	Q	30pF and over	350 min.	10pF and over to under 30pF	275+5/2×C min.	Under 10pF	200+10×C min.	<p>Charge/discharge current shall not exceed 50mA.</p> <p>Leave the capacitor in ambient conditions for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</p>			
	Rated Capacitance	Q											
	30pF and over	350 min.											
10pF and over to under 30pF	275+5/2×C min.												
Under 10pF	200+10×C min.												
D.F. (Class 2)	<p>Characteristics</p> <p>X5R: 200% of initial spec. max.</p> <p>X7R: 200% of initial spec. max.</p>	<p>Voltage conditioning:</p> <p>Voltage treats the capacitor under testing temperature and voltage for 1 hour.</p>											
Insulation Resistance	<p>1,000MΩ or min.</p> <p>(As for the capacitors of rated voltage 16, 10, 6.3V DC, 10MΩ·μF min.,)</p>	<p>Leave the capacitor in ambient conditions for 24±2h before measurement.</p> <p>Use this measurement for initial value.</p>											

*As for the initial measurement of capacitors (Class2) on number 8, 11, 12 and 13, leave capacitor at 150 –10, 0°C for 1 hour and measure the value after leaving capacitor for 24±2h in ambient condition.

Appendix 1

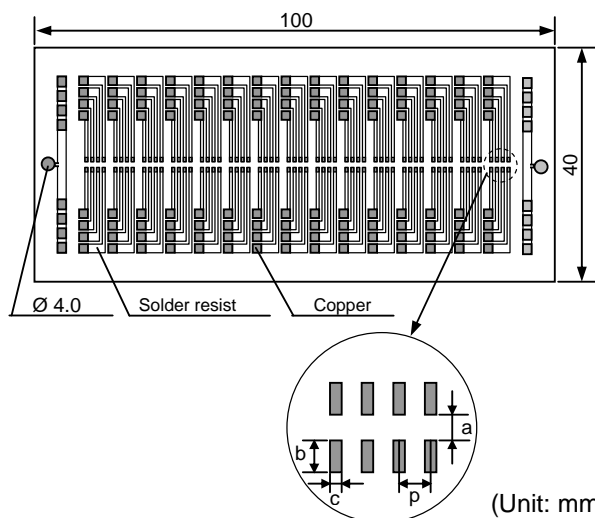
CKCM25, CKCL22



(Unit: mm)

Appendix 2

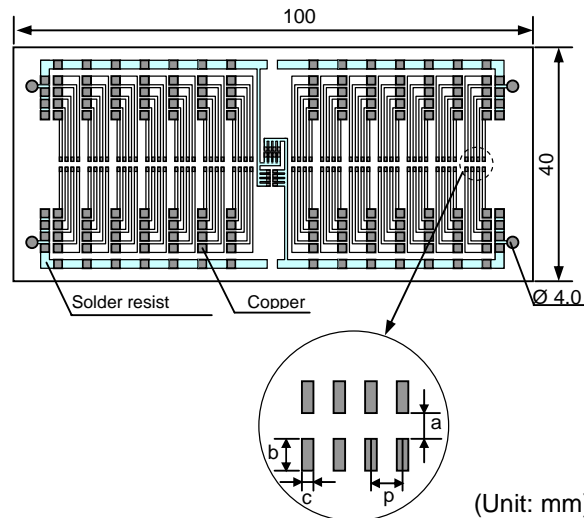
CKCL44



(Unit: mm)

Appendix 3

CKCA43



(Unit: mm)

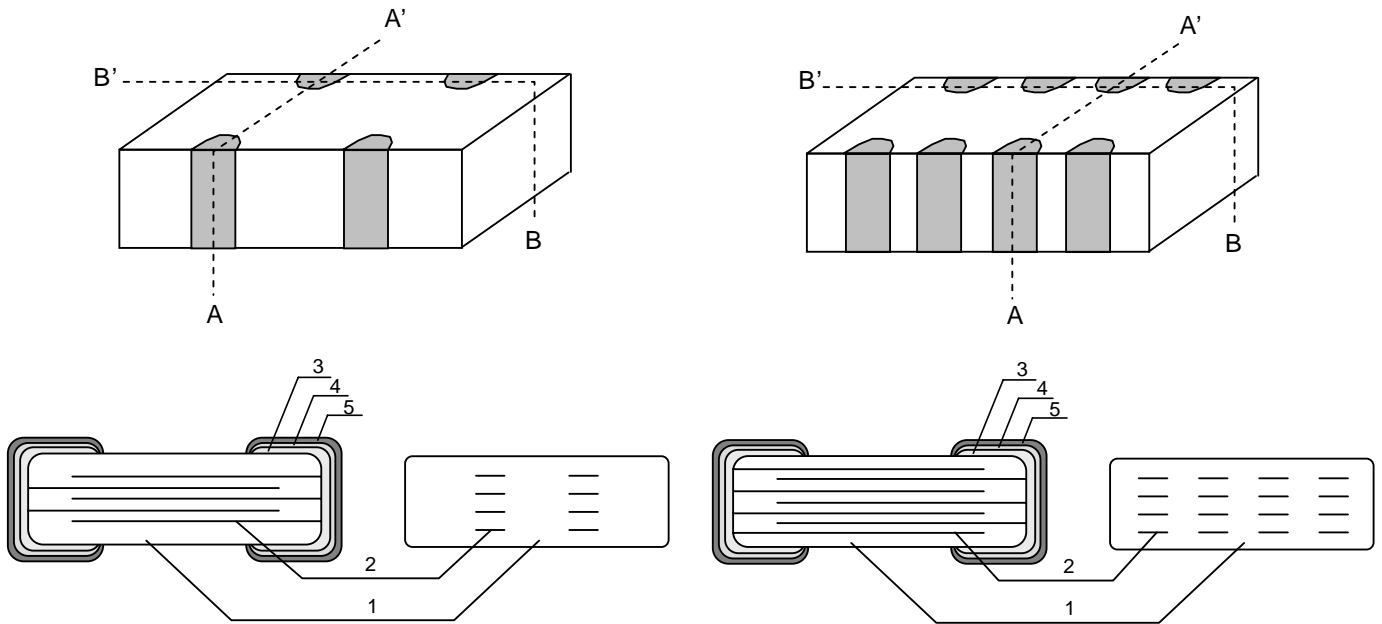
Material: Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness: 1.6mm

- Copper (thickness 0.035mm)
- Solder resist

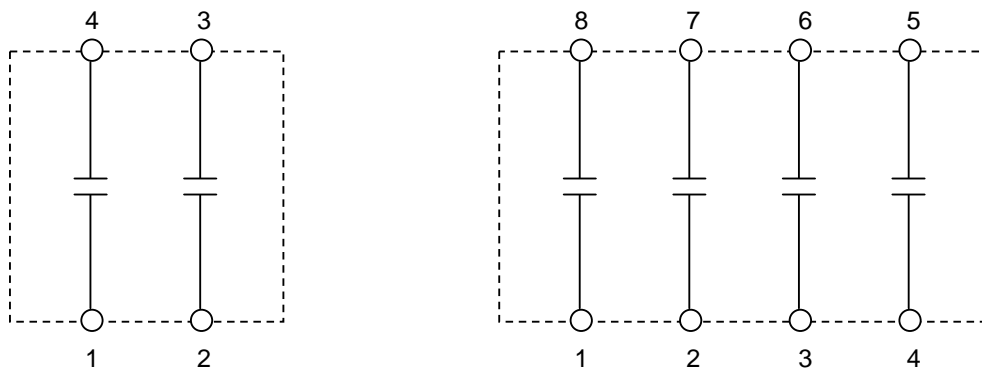
TDK (EIA style)	Dimensions (mm)			
	a	b	c	p
CKCM25	0.5	0.5	0.36	0.64
CKCL22	0.6	0.6	0.45	1.0
CKCL44	0.6	0.7	0.2	0.5
CKCA43	1.0	0.7	0.3	0.8

8. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL	
		Class 1	Class 2
1	Dielectric	CaZrO ₃	BaTiO ₃
2	Electrode	Nickel (Ni)	
3	Termination	Copper (Cu)	
4		Nickel (Ni)	
5		Tin (Sn)	

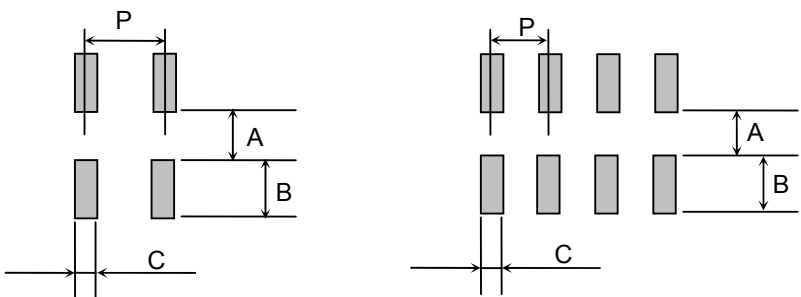
9. EQUIVALENT CIRCUIT



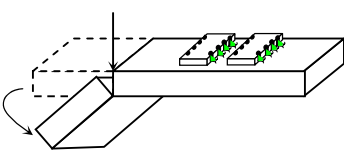
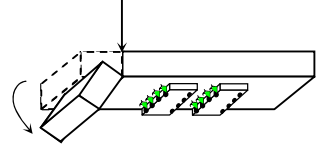
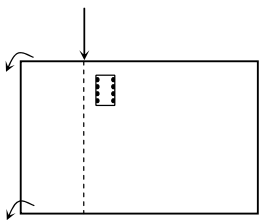
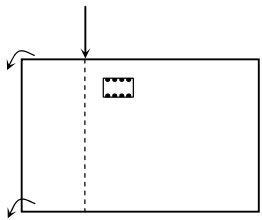
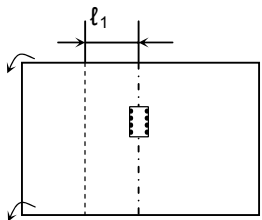
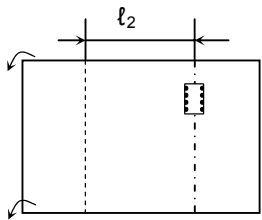
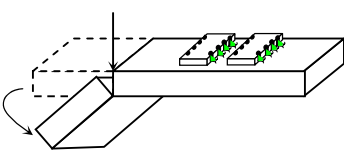
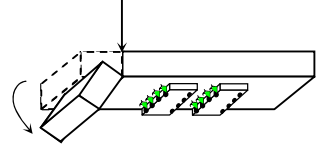
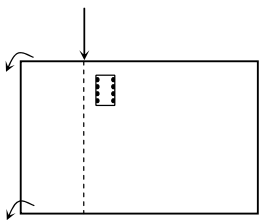
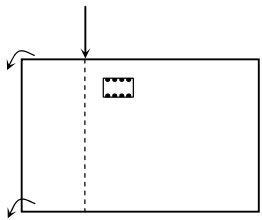
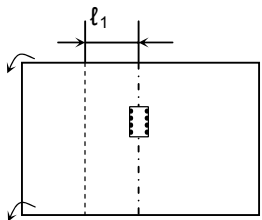
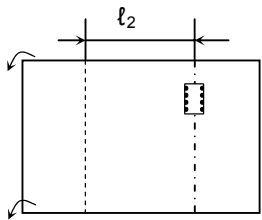
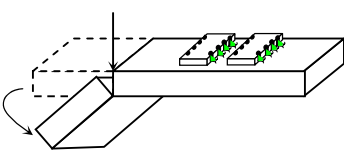
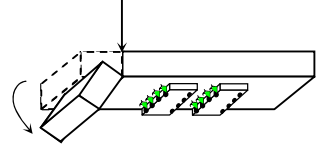
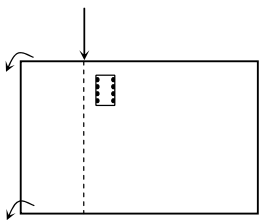
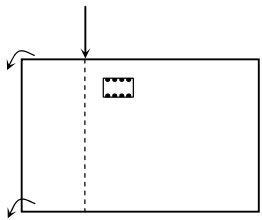
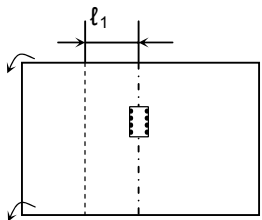
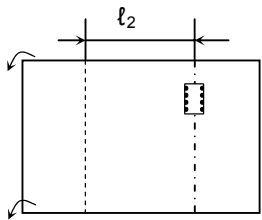
10. Caution

No.	Process	Condition														
1	Operating Condition (Storage, Transportation)	<p>1.1 Storage</p> <ol style="list-style-type: none"> The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt. The capacitor must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur. Avoid storing in sun light and falling of dew. Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability. Capacitor should be tested for solderability when stored for long periods of time. <p>1.2 Handling in transportation</p> <p>In case of the transportation, the performance of the capacitor may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 "Handling in Transportation")</p>														
2	Circuit design	<p>2.1 Operating temperature</p> <p>Operating temperature should be followed strictly within this specification.</p> <ol style="list-style-type: none"> Do not use capacitors above the maximum allowable operating temperature. Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product it's mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) The electrical characteristics of the capacitor will vary depending on the temperature. The capacitor should be selected and designed after taking temperature into consideration. <p>2.2 Operating voltage</p> <ol style="list-style-type: none"> Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. (Reference figures 1 and 2 below). AC or pulse with overshooting, V_{P-P} must be below the rated voltage. (Reference figures 3, 4, and 5 below). When the voltage is started/stopped to apply to the circuit an irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within its rated voltage during these Irregular voltage periods. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Voltage</th> <th style="width: 25%;">(1) DC voltage</th> <th style="width: 25%;">(2) DC+AC voltage</th> <th style="width: 30%;">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Positional Measurement (Rated voltage)</td> <td style="text-align: center;"> </td> <td style="text-align: center;"> </td> <td style="text-align: center;"> </td> </tr> </tbody> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 20%;">Voltage</th> <th style="width: 40%;">(4) Pulse voltage (A)</th> <th style="width: 40%;">(5) Pulse voltage (B)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Positional Measurement (Rated voltage)</td> <td style="text-align: center;"> </td> <td style="text-align: center;"> </td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)	Positional Measurement (Rated voltage)		
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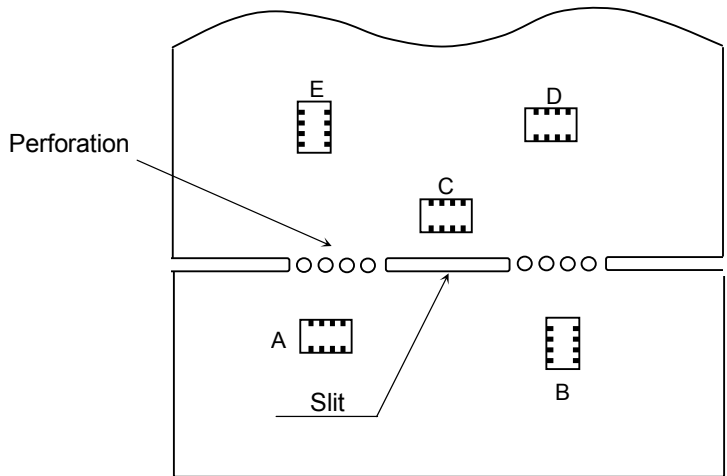
(10. Caution, continued)

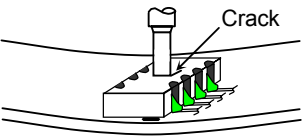
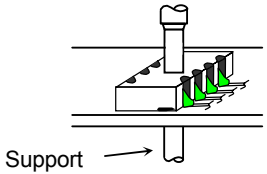
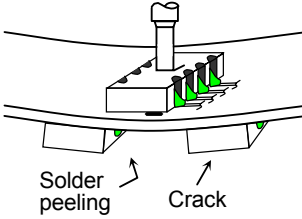
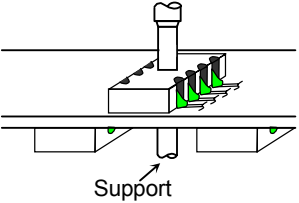
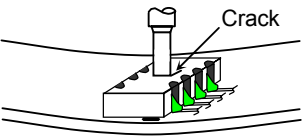
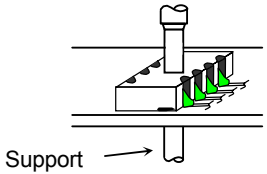
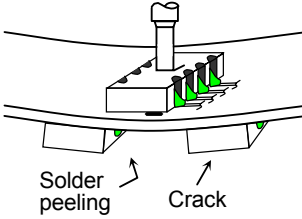
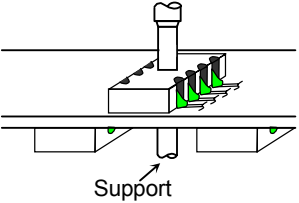
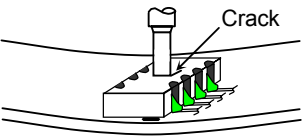
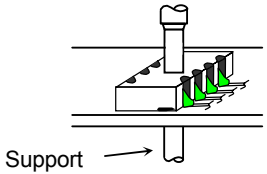
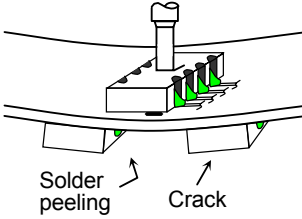
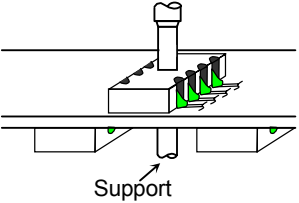
No.	Process	Condition																									
2	Circuit design	<p>2.2 Operating Voltage (continued)</p> <p>2. Even below the rated voltage, if repetitive high AC frequency or pulsed voltage is applied, the reliability of the capacitors may be reduced.</p> <p>3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitor should be selected after considering the voltage affect.</p> <p>2.3 Frequency</p> <p>When Class 2 capacitors are used in AC and/or pulsed voltages, the capacitor may self vibrate and generate audible sound (piezoelectric affect).</p>																									
3[Designing P.C. Board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitor.</p> <p>1. The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.</p> <p>2. Avoid using common solder land for multiple terminations and provide individual solder land for each termination instead.</p> <p>3. Size and recommended land dimensions provided below:</p> <div style="text-align: center;">  </div> <p style="text-align: right;">(mm)</p> <table border="1" data-bbox="560 1123 1438 1375"> <thead> <tr> <th>Type Symbol</th> <th>CKCM25</th> <th>CKCL22</th> <th>CKCL44</th> <th>CKCA43</th> </tr> </thead> <tbody> <tr> <td>P</td> <td>0.64</td> <td>1.0</td> <td>0.5</td> <td>0.8</td> </tr> <tr> <td>A</td> <td>0.3</td> <td>0.4</td> <td>0.55</td> <td>0.6 - 0.7</td> </tr> <tr> <td>B</td> <td>0.45</td> <td>0.6</td> <td>0.6</td> <td>0.8 - 1.0</td> </tr> <tr> <td>C</td> <td>0.3</td> <td>0.5</td> <td>0.25</td> <td>0.4</td> </tr> </tbody> </table>	Type Symbol	CKCM25	CKCL22	CKCL44	CKCA43	P	0.64	1.0	0.5	0.8	A	0.3	0.4	0.55	0.6 - 0.7	B	0.45	0.6	0.6	0.8 - 1.0	C	0.3	0.5	0.25	0.4
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(10. Caution, continued)

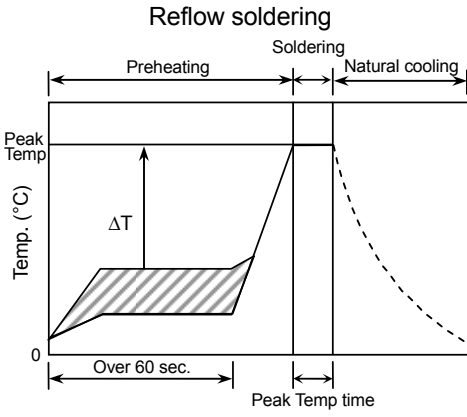
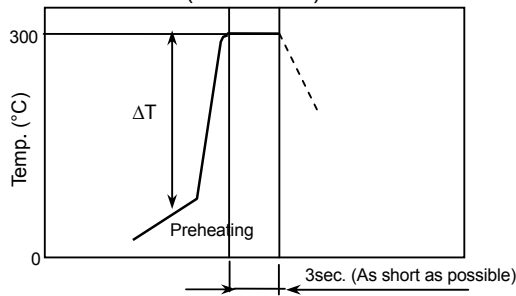
No.	Process	Condition												
3	Designing P.C. Board	<p>4) Recommended chip capacitors layout is provided below:</p> <table border="1"> <thead> <tr> <th data-bbox="506 235 683 310"></th> <th data-bbox="683 235 1040 310">Disadvantage against bending stress</th> <th data-bbox="1040 235 1398 310">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="506 310 683 701">Mounting face</td> <td data-bbox="683 310 1040 701"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p> </td> <td data-bbox="1040 310 1398 701"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="506 701 683 1121">Chip arrangement (Direction)</td> <td data-bbox="683 701 1040 1121"> <p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p>  </td> <td data-bbox="1040 701 1398 1121"> <p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="506 1121 683 1570">Distance from slit</td> <td data-bbox="683 1121 1040 1570"> <p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p> </td> <td data-bbox="1040 1121 1398 1570"> <p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p>	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p>	Chip arrangement (Direction)	<p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p> 	<p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p> 	Distance from slit	<p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p>	<p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p>
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(10. Caution, continued)

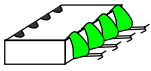
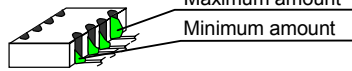
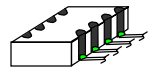
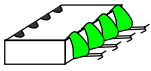
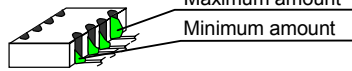
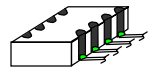
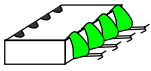
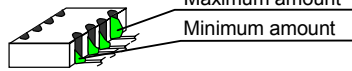
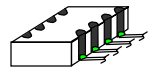
No.	Process	Condition
3	Designing P.C. Board	<p data-bbox="422 161 1356 199">5) Mechanical stress varies according to location of chip capacitor on the P.C. board.</p> <div data-bbox="479 252 1201 724"><p>The diagram illustrates a cross-section of a PCB with a central layer containing a row of four circular holes. Above this layer, capacitor E is positioned directly over the first hole, capacitor C is centered over the second hole, capacitor D is positioned over the third hole, and capacitor B is positioned over the fourth hole. Below the central layer, capacitor A is positioned over the first hole, and capacitor B is positioned over the fourth hole. A horizontal slit is shown below the central layer, and a perforation is shown above it. Arrows point from the labels 'Perforation' and 'Slit' to their respective features.</p></div> <p data-bbox="470 745 1388 808">The relative stress applied to these capacitors during depaneling is in the following order:</p> $A > B = C > D > E$

No.	Process	Condition									
4	Mounting	<p>4.1 Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitor and result in cracking. Please take following precautions.</p> <ol style="list-style-type: none"> 1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface but not contact it. 2. Adjust the mounting head pressure to be 1 to 3N of static weight. 3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board. <p>See following examples.</p> <table border="1" data-bbox="516 558 1403 1087"> <thead> <tr> <th data-bbox="516 558 686 606"></th> <th data-bbox="686 558 1057 606">Not recommended</th> <th data-bbox="1057 558 1403 606">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="516 606 686 840">Single sided mounting</td> <td data-bbox="686 606 1057 840">  </td> <td data-bbox="1057 606 1403 840">  </td> </tr> <tr> <td data-bbox="516 840 686 1087">Double-sides mounting</td> <td data-bbox="686 840 1057 1087">  </td> <td data-bbox="1057 840 1403 1087">  </td> </tr> </tbody> </table> <p>When the centering jaw is worn, mechanical impact on the capacitor may occur and damage the product. Please control the closing dimension of the centering jaw and provide sufficient preventive maintenance and/or replacement of necessary.</p>		Not recommended	Recommended	Single sided mounting			Double-sides mounting		
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Double-sides mounting											

(10. Caution, continued)

No.	Process	Condition														
5	Soldering	<p>5.1 Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, the following recommended:</p> <ol style="list-style-type: none"> 1. Use a mildly activated rosin flux (less than 0.1wt% chlorine). 2. Excessive flux must be avoided. Please provide proper amount of flux. 3. When water-soluble flux is used, sufficient washing is necessary. <p>5.2 Recommended soldering profile by various methods</p> <div style="text-align: center;"> <p>Reflow soldering</p>  </div> <div style="text-align: center; margin-top: 20px;"> <p>Manual soldering (Solder iron)</p>  </div> <p>5.3 Recommended soldering peak temp and duration</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th rowspan="2" style="text-align: center;">Temp./Duration</th> <th colspan="2" style="text-align: center;">Reflow soldering</th> </tr> <tr> <th style="text-align: center;">Peak temp(°C)</th> <th style="text-align: center;">Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Solder</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">Sn-Pb Solder</td> <td style="text-align: center;">230 max.</td> <td style="text-align: center;">20 max.</td> </tr> <tr> <td style="text-align: center;">Lead Free Solder</td> <td style="text-align: center;">260 max.</td> <td style="text-align: center;">10 max.</td> </tr> </tbody> </table> <p>Recommended solder compositions Sn-37Pb (Sn-Pb solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>	Temp./Duration	Reflow soldering		Peak temp(°C)	Duration(sec.)	Solder			Sn-Pb Solder	230 max.	20 max.	Lead Free Solder	260 max.	10 max.
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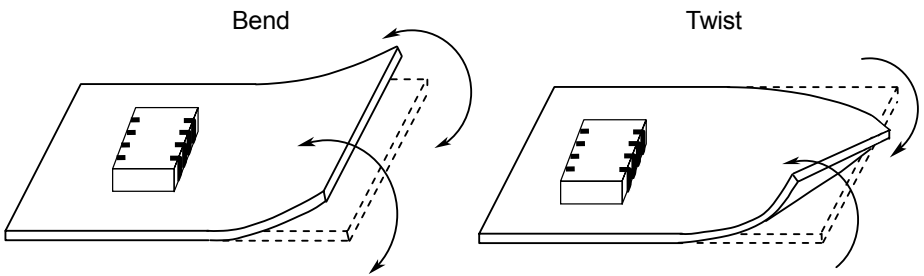
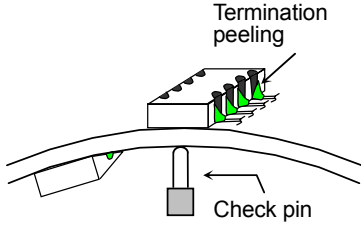
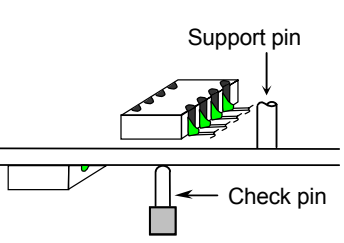
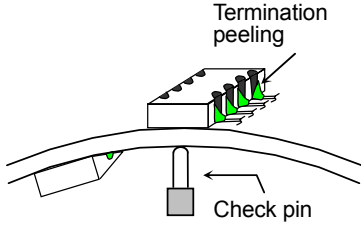
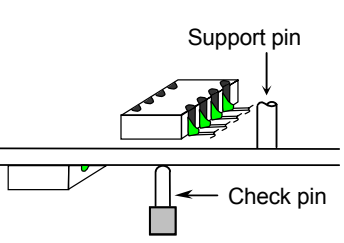
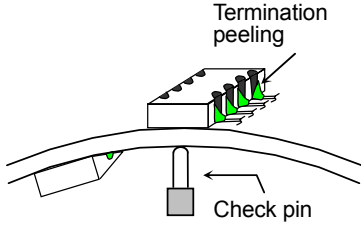
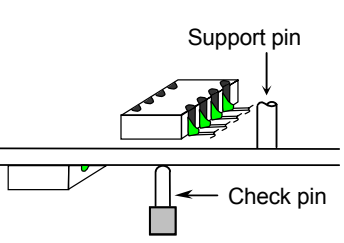
(10. Caution, continued)

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5	Soldering (continued)	<p>5.4 Avoiding thermal shock</p> <p>1. Preheating condition</p> <table border="1" data-bbox="581 247 1333 449"> <thead> <tr> <th data-bbox="581 247 797 338" rowspan="2">Soldering</th> <th colspan="2" data-bbox="797 247 1333 289">Temp. (°C)</th> </tr> <tr> <th data-bbox="797 289 1141 338">CKCM25, CKCL22, CKCL44</th> <th data-bbox="1141 289 1333 338">CKCA43</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 338 797 394">Reflow soldering</td> <td data-bbox="797 338 1141 394">$\Delta T \leq 150$</td> <td data-bbox="1141 338 1333 394">$\Delta T \leq 130$</td> </tr> <tr> <td data-bbox="581 394 797 449">Manual soldering</td> <td data-bbox="797 394 1141 449">$\Delta T \leq 150$</td> <td data-bbox="1141 394 1333 449">$\Delta T \leq 130$</td> </tr> </tbody> </table> <p>2. Cooling condition</p> <p>Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.</p> <p>5.5 Amount of solder</p> <p>Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. In sufficient solder may detach the capacitor from the P.C. board.</p> <table border="0" data-bbox="529 814 1414 1226"> <tr> <td data-bbox="529 814 721 940">Excessive solder</td> <td data-bbox="721 814 1105 940">  </td> <td data-bbox="1105 814 1414 940">Higher tensile force on the chip capacitor may cause cracking.</td> </tr> <tr> <td data-bbox="529 940 721 1073">Adequate solder</td> <td data-bbox="721 940 1105 1073">  </td> <td></td> </tr> <tr> <td data-bbox="529 1073 721 1226">Insufficient solder</td> <td data-bbox="721 1073 1105 1226">  </td> <td data-bbox="1105 1073 1414 1226">Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.</td> </tr> </table> <p>5.6 Solder repair by solder iron</p> <p>1. Selection of the soldering iron tip</p> <p>Tip temperatures of solder iron varies by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation. However, heat shock may cause a crack in the chip capacitor. Please confirm the tip temperature. before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)</p> <p>Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)</p> <table border="1" data-bbox="581 1598 1365 1703"> <thead> <tr> <th data-bbox="581 1598 781 1654">Temp. (°C)</th> <th data-bbox="781 1598 976 1654">Duration (sec.)</th> <th data-bbox="976 1598 1170 1654">Wattage (W)</th> <th data-bbox="1170 1598 1365 1654">Shape (mm)</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 1654 781 1703">300 max.</td> <td data-bbox="781 1654 976 1703">3 max.</td> <td data-bbox="976 1654 1170 1703">20 max.</td> <td data-bbox="1170 1654 1365 1703">Ø 3.0 max.</td> </tr> </tbody> </table>	Soldering	Temp. (°C)		CKCM25, CKCL22, CKCL44	CKCA43	Reflow soldering	$\Delta T \leq 150$	$\Delta T \leq 130$	Manual soldering	$\Delta T \leq 150$	$\Delta T \leq 130$	Excessive solder		Higher tensile force on the chip capacitor may cause cracking.	Adequate solder			Insufficient solder		Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.	Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	Ø 3.0 max.
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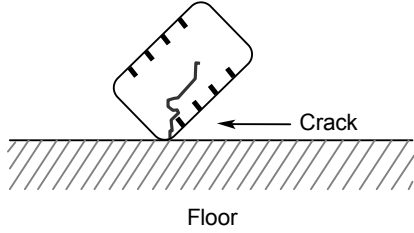
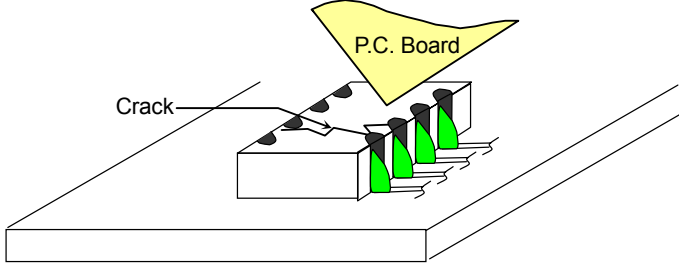
(10. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	<p>2. Direct contact of the soldering iron with ceramic dielectric of chip the capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5.7 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5.8 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 "Recommendations to prevent the tombstone phenomenon")</p>
6	Cleaning	<p>1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and deteriorate the insulation resistance.</p> <p>2. If cleaning condition is not suitable, it may deteriorate the chip capacitor's insulation resistance.</p> <p>2.1 Insufficient washing</p> <ol style="list-style-type: none">1. Terminal electrodes may be corroded by Halogen in the flux.2. Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance.3. Water soluble flux has higher tendency to have above mentioned problems (1) and (2). <p>2.2 Excessive washing</p> <p>When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended.</p> <p style="text-align: center;">Power: 20 W/ ℓmax. Frequency: 40 kHz max. Washing time: 5 minutes max.</p> <p>2.3 If the cleaning fluid is contaminated, of Halogen concentration can increase, may bring the same result as insufficient cleaning.</p>

(10. Caution, continued)

No.	Process	Condition						
7	Coating and molding of the P.C. Board	<ol style="list-style-type: none"> When the P.C. board is coated, please verify the impact on the capacitor. Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor. Please verify the curing temperature. 						
8	Handling after chip mounted	<ol style="list-style-type: none"> Please pay attention not to bend or distort the P.C. board after soldering otherwise the chip capacitor may crack. <div style="text-align: center; margin: 10px 0;">  </div> When functional check of the P.C. board is performed, high pin pressure tends to be used for fear of loose contact. But if the pressure is excessive and bends the P.C. board, it may crack the chip capacitor or peel the termination. Please adjust the pins accordingly to ensure the P.C. board is not flexed. <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th data-bbox="527 1039 657 1092">Item</th> <th data-bbox="657 1039 1047 1092">Not recommended</th> <th data-bbox="1047 1039 1421 1092">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="527 1092 657 1375" style="text-align: center; vertical-align: middle;">Board bending</td> <td data-bbox="657 1092 1047 1375" style="text-align: center;">  </td> <td data-bbox="1047 1092 1421 1375" style="text-align: center;">  </td> </tr> </tbody> </table> 	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								

(10. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitors	<p>1. The chip capacitor may crack, if dropped, especially large case sizes. Please handle with care and do not use if dropped.</p>  <p>2. When stacking the P.C. board for storage or handling after soldering, the corner of the P.C. board may hit the chip capacitor of a neighboring board a cause crack.</p> 
10	Capacitance aging	Class 2 capacitors have an aging characteristic, which is a decrease capacitance over time due to crystalline changes that occur in ferroelectric ceramics. Careful consideration should be done in case of a time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life and (failure rate) depend on the temperature and voltage applied. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 "Calculation of the estimated lifetime and the failure rate." The risk can be decreased by reducing the temperature and voltage but it will not be guaranteed.
12	Others	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet:</p> <p>Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, ships, etc.) Medical equipment. Power-generation control equipment. Atomic energy-related equipment. Seabed equipment. Transportation control equipment. Public information-processing equipment. Military equipment. Electric heating apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose applications.</p> <p>When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup circuits, etc., to ensure higher safety.</p>

11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example M 0 A - 00 - 000
 (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

12. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

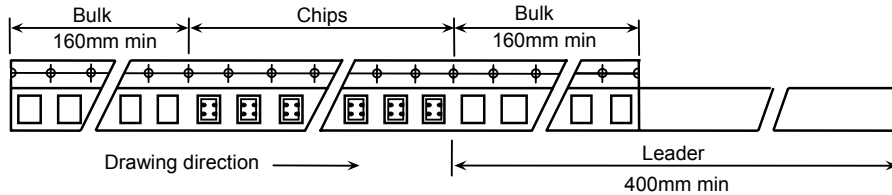
13. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 4.
 Dimensions of plastic tape shall be according to Appendix 5.

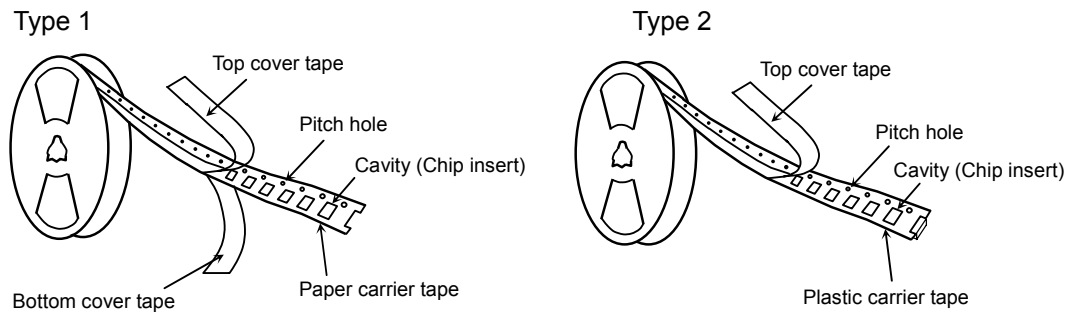
2. Bulk part and leader of taping



3. Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 6.
 Dimensions of Ø330 reel shall be according to Appendix 7.

4. Structure of taping

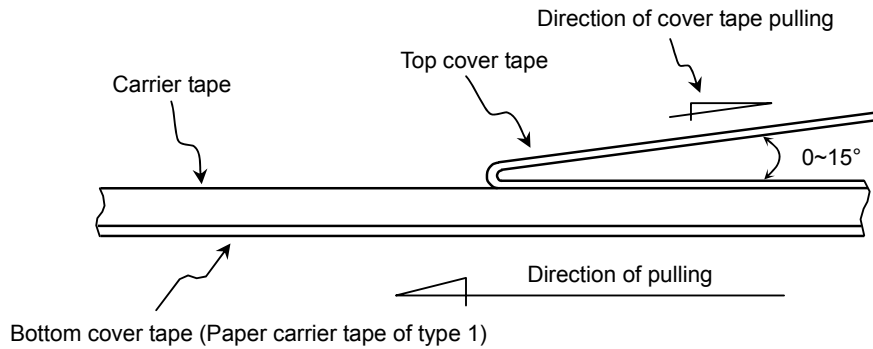


2. CHIP QUANTITY

Type	Taping Material	Chip quantity (pcs.)	
		φ178mm reel	φ330mm reel
CKCM25	Paper	4,000	10,000
CKCL22	Plastic		
CKCL44	Paper		
CKCA43	Plastic	2,000	

3. PERFORMANCE SPECIFICATIONS

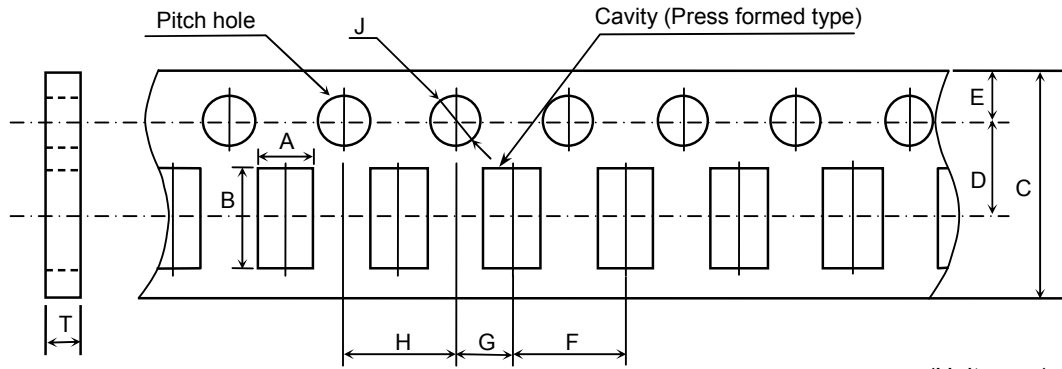
1. Peel back cover (top tape)
0.05-0.7N. (See the following figure.)



2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.
3. The missing of components shall be less than 0.1%
4. Components shall not stick to the cover tape.
5. The cover tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 4

Paper Tape



(Unit: mm)

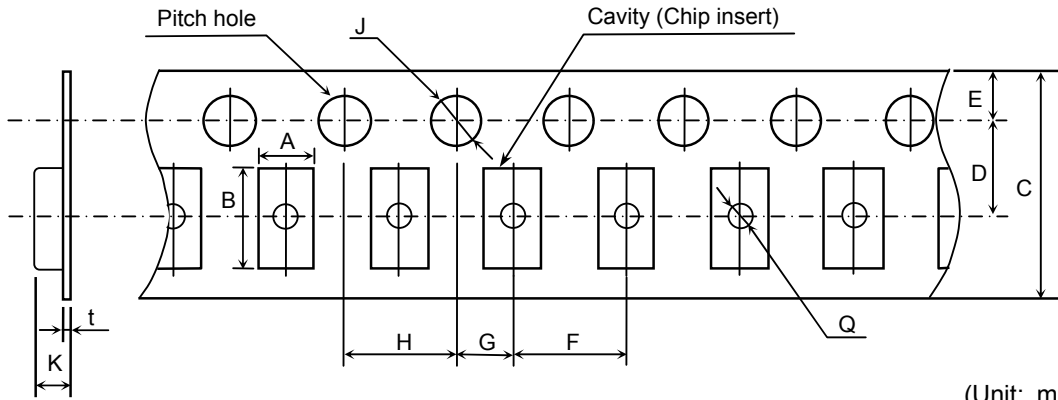
Symbol Type	A	B	C	D	E	F
CKCM25	(1.30)	(1.70)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
CKCL44	(1.50)	(2.30)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10

Symbol Type	G	H	J	T
CKCM25	2.00 ± 0.05	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	1.10 max.
CKCL44	2.00 ± 0.05	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	1.10 max.

* The values in the parentheses () are for reference.

Appendix 5

Plastic Tape



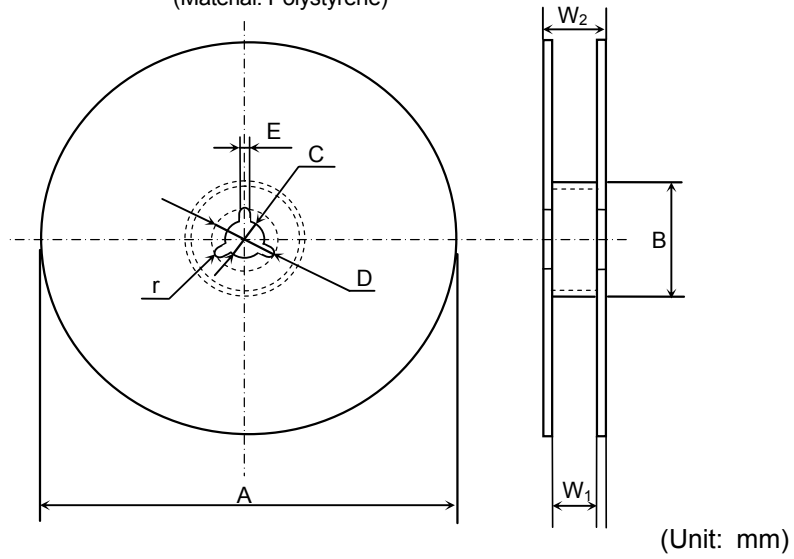
(Unit: mm)

Symbol Type	A	B	C	D	E	F
CKCL22	(1.50)	(2.30)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
CKCA43	(1.90)	(3.50)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
Symbol Type	G	H	J	K	t	Q
CKCL22	2.00 ± 0.05	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	2.50 max.	0.30 max.	∅ 0.50 min.
CKCA43	2.00 ± 0.05	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	2.50 max.	0.30 max.	∅ 0.50 min.

* The values in the parentheses () are for reference.

Appendix 6

(Material: Polystyrene)

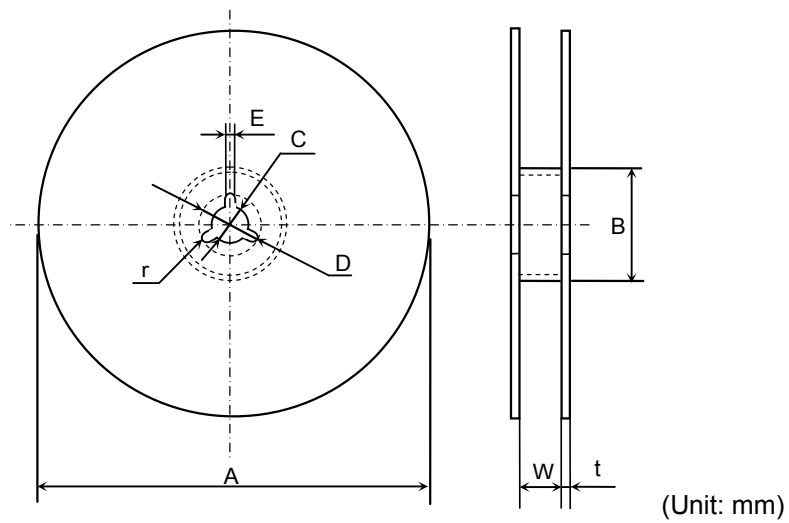


(Unit: mm)

Symbol	A	B	C	D	E	W ₁
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3
Symbol	W ₂	r				
Dimension	13.0 ± 1.4	1.0				

Appendix 7

(Material: Polystyrene)



(Unit: mm)

Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5
Symbol	t	r				
Dimension	2.0 ± 0.5	1.0				

END PAGE