SPECIFICATION

SPEC. No.

DATE :

Customer

CUSTOMER’S PRODUCT NAME	TDK PRODUCT NAME MULTILAYER CERAMIC CHIP CAPACITORS CKD710JB, CKD610JB, CKD510JB, CKD110JB, CKD310JB Type(Low ESL Feed Trough)

Please sign return this specification to TDK representatives. If orders are placed without this returned documentation, we must consider you found the specification acceptable.

THIS SPECIFICATION IS RECEIVED

DATE: YEAR MONTH DAY

TDK-EPC Corporation
1-13-1, Nihonbashi, Chuo-ku, Tokyo
103-0027, Japan

ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office

Sales Tel. ( )

PRODUCT CLASSIFICATION CODE	040320

REV 0.3 / 201012

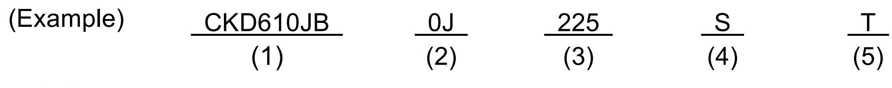
1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK-EPC HONG KONG LIMITED, TDK (Suzhou) Co., Ltd, TDK (Malaysia) Sdn. Bhd and TDK Components U.S.A. Inc.

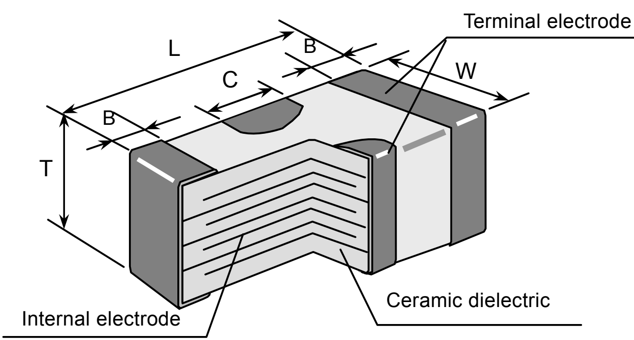
EXPLANATORY NOTE:

This specification warrants the quality of the TDK ceramic chip capacitor. The product should be evaluated and confirmed in your product before use. If the use of the product exceeds the bounds of the specification, we can not guarantee its quality and/or reliability.

2. CODE CONSTRUCTION



1. Type



Please refer to product list for the dimension of each product. See Section 8 for inside structure and material.

2. Rated Voltage

Symbol	Rated Voltage
1 H	50 V DC
1 E	25 V DC
1 C	16 V DC
1 A	10 V DC
0 J	6.3 V DC

3. Rated Capacitance

Stated in three digits and in units of pico farads (pF).The first and second digits identify the first and second significant figure of the capacitance, the third digit identifies the multiplier. R is designated for a decimal point.

Example 225 → 2,200,000pF

4. Capacitance tolerance

See the cap range chart In the TDK Product Guide for this series to obtain item specific parameters.

Symbol	Tolerance
S	+ 50, -20 %
M	±20 %

5. Packaging

Symbol	Packaging
B	Bulk
T	Taping

3. RATED CURRENT

DC2A

DC1A

DC500mA

DC400mA

DC200mA

See the cap range chart In the TDK Product Guide for this series to obtain item specific parameters.

4. OPERATING TEMPERATURE RANGE

-25 ~ 85°C

-55 ~ 85°C

-55 ~ 125°C

See the cap range chart In the TDK Product Guide for this series to obtain item specific parameters

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

6. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

7. PERFORMANCE

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td>External Appearance</td><td>No defects which may affect performance.</td><td>Inspect with magnifying glass (3X)</td></tr>
<tr><td>2</td><td>Insulation Resistance</td><td>10,000MΩ or 500MΩ·μF min. whichever smaller (As for the capacitors of rated voltage 16, 10, 6.3V DC, 100MΩ·μF min.).</td><td>Apply rated voltage for 60s.</td></tr>
<tr><td>3</td><td>Direct Current Resistance
$R_{dc\ (1-2)}$</td><td>R_{dc} is between 5MΩ - 600 MΩ depending on item. See the cap range chart in the TDK Product Guide for this series to obtain item specific parameters.</td><td>Measuring current should be 100mA max.
3
1
2
4</td></tr>
<tr><td>4</td><td>Voltage Proof</td><td>Withstand test voltage without insulation breakdown or other damage.</td><td>2.5 times of rated voltage.
Above DC voltage shall be applied for 1 to 5s.
Charge / discharge current shall not exceed 50mA.</td></tr>
<tr><td>5</td><td>Capacitance</td><td>Within the specified capacitance tolerance.</td><td><table><tr><th>Measuring frequency</th><th>Measuring voltage</th></tr><tr><td rowspan="2">1kHz±10%</td><td>0.5±0.2Vrms.</td></tr><tr><td>1.0±0.2Vrms.</td></tr></table></td></tr>
<tr><td>6</td><td>Dissipation Factor (DF)</td><td>Max. DF= 0.10</td><td>See No.5 in this table for measuring condition.</td></tr>
</table>

(7. Performance, continued)

No.	Item		Performance	Test or inspection method
7	Bending		No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 2, Appendix 4 or Appendix 6) and bend 1mm. 20, 50, F, R230, 1, 45, 45 (Unit: mm)
8	Solderability		New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of “A sections” shall not be exposed due to melting or shifting of termination material. A section	Completely soak both terminations in solder at 235±5°C for 2±0.5s. Solder: H63A (JIS Z 3282) Flux: Isopropyl alcohol (JIS K 8839) Rosin(JIS K 5902) 25% solid solution.
9	Resistance to solder heat	External appearance	No mechanical damage.	Completely soak both terminations in solder at 260±5°C for 5±1s. Preheating condition Temp.: 150±10°C Time: 1 to 2min. Flux: Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution. Solder: H63A (JIS Z 3282) Leave the capacitor in ambient conditions for 24±2h before measurement.
		Capacitance	Change from the value before test ± 7.5 %	
		D.F.	Meet the initial spec.	
		Insulation Resistance	Meet the initial spec.	
		Voltage proof	No insulation breakdown or other damage.	
		Resistance for DC R_{dc}	1.0 Ω max.	

(7. Performance, continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="5">10</td><td rowspan="5">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitor on P.C. board (shown in Appendix 1 or Appendix 3) before testing.

Expose the capacitor in the conditions step1 through step 4 and repeat 5 times consecutively.

Leave the capacitor in ambient conditions for 24±2h before measurement.
<table><tr><th>Step</th><th>Temperature(°C)</th><th>Time (min.)</th></tr><tr><td>1</td><td>Min. operating temp. ± 3</td><td>30 ± 3</td></tr><tr><td>2</td><td>20 ± 2</td><td>2 - 5</td></tr><tr><td>3</td><td>Max. operating temp. ± 2</td><td>30 ± 2</td></tr><tr><td>4</td><td>20 ± 2</td><td>2 - 5</td></tr></table></td></tr>
<tr><td>Capacitance</td><td>Change from the value before test
± 7.5 %</td></tr>
<tr><td>D.F.</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Resistance for DC R_{dc}</td><td>1.0Ω max.</td></tr>
<tr><td rowspan="5">11</td><td rowspan="5">Moisture Resistance (Steady State)</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on P.C. board (shown in Appendix 1 or Appendix 3) before testing.

Leave at temperature 40±2°C, 90 to 95%RH for 500 +24,0h.

Leave the capacitor in ambient conditions for 24±2h before measurement.</td></tr>
<tr><td>Capacitance</td><td>Change from the value before test
± 12.5 %</td></tr>
<tr><td>D.F.</td><td>Characteristics
200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>1,000MΩ or 50MΩ·μF min. whichever smaller. (As for the capacitors of rated voltage 16, 10, 6.3V DC, 10MΩ·μF min.,)</td></tr>
<tr><td>Resistance for DC R_{dc}</td><td>1.0 Ω max.</td></tr>
</table>

(7. Performed, continued)

No.	Item		Performance	Test or inspection method
12	Life	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1, Appendix 3 or Appendix 5) before testing. Below the voltage shall be applied at maximum operating temperature ±2°C for 1,000 +48, 0h. Applied voltage is 1xRV; however some items may be tested at higher voltage (1.2x, 1.5x or 2xRV). Contact TDK for details. Charge/discharge current shall not exceed 50mA. Leave the capacitor in ambient conditions for 24±2h before measurement. Voltage conditioning: Voltage treats the capacitor under testing temperature and voltage for 1 hour. Leave the capacitor in ambient conditions for 24±2h before measurement. Use this measurement for initial value.
		Capacitance	Change from the value before test ± 15 %	
		D.F.	Characteristics 200% of initial spec. max.	
		Insulation Resistance	1,000MΩ or 50MΩ·μF min. whichever smaller. (As for the capacitors of rated voltage 16, 10, 6.3V DC, 10MΩ·μF min.,)	
		Resistance for DC R_{dc}	1.0 Ω max.	

*As for the initial measurement of capacitors on number 9, 10 and 11, leave capacitors at 150 –10, 0°C for 1 hour and measure the value after leaving capacitors for 24±2h in ambient condition.

Appendix - 1

P.C. Board for reliability test

100

4

Solder resist

Copper

(Unit: mm)

Appendix - 2

P.C. Board for bending test

100

40

Solder resist

Copper

(Unit: mm)

c

f

d

e

f

b a b

TDK (EIA style)	Dimensions (mm)					
	a	b	c	d	e	f
CKD710JB	0.7	0.3	0.19	0.6	0.25	0.25

1. Material: Glass Epoxy (As per JIS C6484 GE4)

2.Thickness：1.6mm

Copper(Thickness　0.035mm)

Solder resist

Appendix - 3

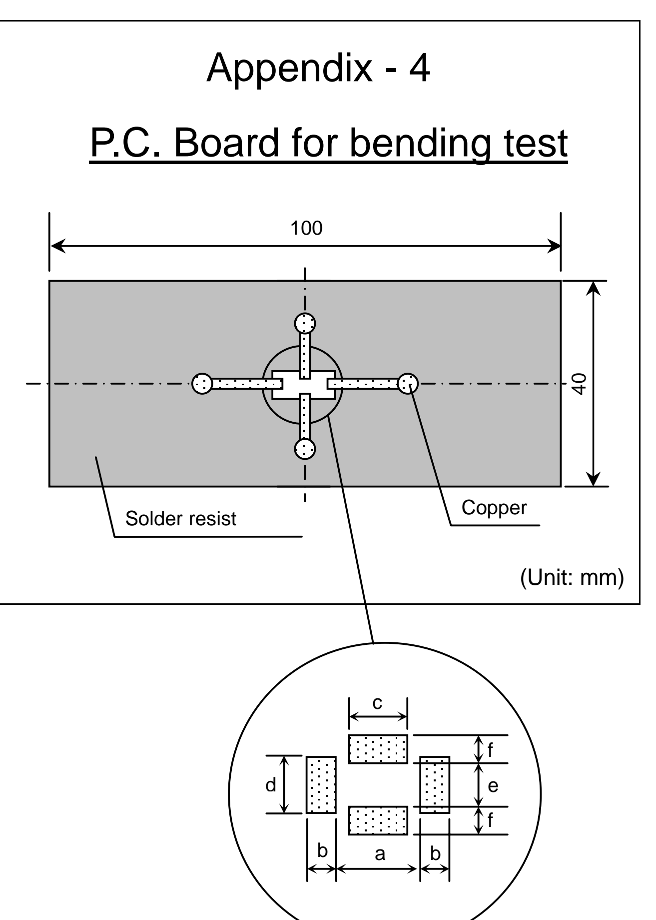
<u>P.C. Board for reliability test</u>

100

40

(Unit: mm)

c c d b a b



Appendix - 3

TDK (EIA style)	Dimensions (mm)					
	a	b	c	d	e	f
CKD610JB	1.0	0.6	0.4	0.6	0.4	0.4

Appendix - 4

TDK (EIA style)	Dimensions (mm)			
	a	b	c	d
CKD610JB	0.4	0.5	0.4	2.0

1. Material: Glass Epoxy (As per JIS C6484 GE4)

2.Thickness：1.6mm

Copper(Thickness 0.035mm)

Solder resist

Appendix - 5

P.C. Board for reliability test

100

40

(Unit: mm)

Appendix - 6

P.C. Board for bending test

100

40

Copper

Solder resist

(Unit: mm)

c

f

e

f

d

b a b

TDK (EIA style)	Dimensions (mm)					
	a	b	c	d	e	f
CKD510JB	1.4	0.6	0.5	0.8	0.6	0.65
CKD110JB	2.5	0.7	1.4	1.0	0.6	0.7
CKD310JB	2.5	1.2	1.4	1.3	0.8	0.9

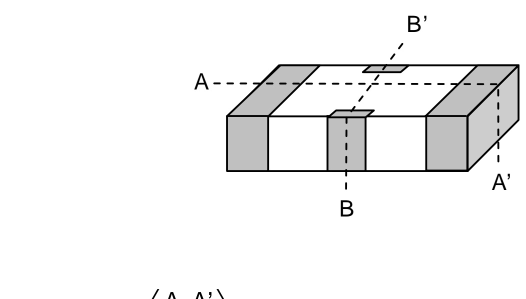
1. Material: Glass Epoxy (As per JIS C6484 GE4)

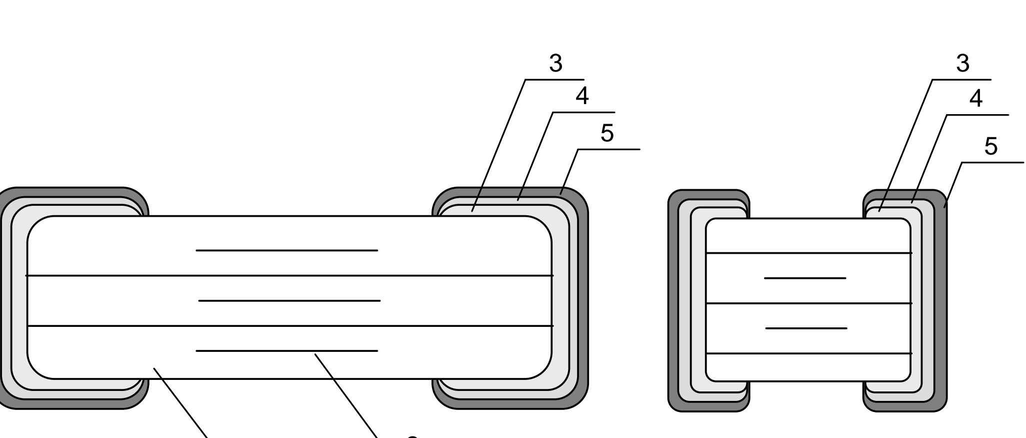
2.Thickness：1.6mm

Copper(Thickness 0.035mm)

Solder resist

8. INSIDE STRUCTURE AND MATERIAL





No.	NAME	MATERIAL
1	Dielectric	$CaZrO_3$ or $BaTiO_3$
2	Electrode	Nickel (Ni)
3	Termination	Copper (Cu)
4		Nickel (Ni)
5		Tin (Sn)

9. Caution

No.	Process	Condition
1	Operating Condition (Storage, Transportation)	1.1 Storage 1. The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt. 2. The capacitors must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur. 3. Avoid storing in sun light and falling of dew. 4. Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability. 5. Capacitors should be tested for the solderability when they are stored for long periods of time. 1.2 Handling in transportation In case of the transportation the performance of the capacitor may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 “Handling in Transportation”)
2	Circuit design	2.1 Operating temperature Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature. 1. Do not use capacitors above the maximum allowable operating temperature. 2. Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product its mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) 3. The electrical characteristics of the capacitors will vary depending on the temperature. The capacitors should be selected and designed after taking the temperature into consideration. 2.2 Operating voltage 1. Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V0-P must be below the rated voltage. Reference figures 1 and 2 below. AC or pulse with overshooting, VP-P must be below the rated voltage. Reference: figures 3, 4, and 5 below. When the voltage is started/ stopped to apply to the circuit an irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within its rated voltage during these Irregular voltage periods.

Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage
Positional Measurement (Rated voltage)	V_{0-P} 0	V_{0-P} 0	V_{P-P} 0

Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)
Positional Measurement (Rated voltage)	V_{P-P} 0	V_{P-P} 0

(9. Caution, continued)

No.	Process	Condition
2	Circuit design	2.2 Operating Voltage (continued) 2. Even below the rated voltage, if repetitive high AC frequency or pulsed voltage is applied, the reliability of the capacitors may be reduced. 3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitors should be selected after considering the voltage affect. 2.3 Frequency When Class 2 capacitors are used in AC and/or pulse voltages, the capacitors may self vibrate and generate audible sound (piezoelectric affect).
3	Designing P.C. Board	The amount of solder at the terminations directly impacts the reliability of the capacitor. 1. The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder lands to ensure the proper amount of solder is applied to the terminations. 2. Avoid using common solder land for multiple terminations and provide individual solder land for each termination instead. 3. Size and recommended land dimensions provided below: <CKD710JB> Chip mounted size Through hole φ0.4 ~ 0.6 a, b, c, d, e Resist / Cu pattern / No pattern Back side: Back side shall be connected to the ground pattern of the chip mounted side. Please design the back side ground as large as possible. Connect to the ground pattern of the chip mounted side. Ground pattern *If thorough hole is too large, solder paste may come into the hole and make bad connection with the ground pattern.

(mm)

Symbol \ Type	a	b	c	d	e
CKD710JB	0.19	0.7	1.3	0.6	0.75

(9. Caution, continued)

No.	Process	Condition
3	Designing P.C. Board	<CKD610JB> Chip mounted size

Connect to the ground pattern of the chip mounted side.

"Through hole" should be designed as close to GND terminal as possible.

(mm)

Symbol \ Type	a	b	c	d	e
CKD610JB	0.4	1.2	2.2	0.7	1.4

<CKD510JB, CKD110JB, CKD310JB>

Chip mounted size

Back side:
Back side shall be connected to the ground pattern of the chip mounted side. Please design the back side ground as large as possible.

*If through hole is too big, solder paste may come into the hole and make bad connection with the ground pattern.

(mm)

Symbol \ Type	a	b	c	d	e
CKD510JB	0.5	1.5	2.6	1.0	2.0
CKD110JB	1.4	2.5	4.5	1.0	2.0
CKD310JB	1.4	2.5	4.5	1.2	2.4

No.	Process	Condition
	Designing P.C. Board (continued)	4. Recommended chip capacitor layout is provided below:

	Disadvantage against bending stress	Advantage against bending stress
Mounting face	Perforation or slit Break P.C. board with mounted side up.	Perforation or slit Break P.C. board with mounted side down.
Chip arrangement (Direction)	Mount perpendicularly to perforation or slit Perforation or slit	Mount in parallel with perforation or slit Perforation or slit
Distance from slit	Closer to slit is higher stress ℓ_1 ($\ell_1 < \ell_2$)	Away from slit is less stress ℓ_2 ($\ell_1 < \ell_2$)

(9. Caution, continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>3</td><td>Designing
P.C. Board
(continued)</td><td>5. Mechanical stress varies according to location of chip capacitor on the P.C. board.

Perforation
E D C A B
Slit

The relative stress applied to these capacitors during depaneling is in the following order:
A > B = C > D > E</td></tr>
<tr><td>4</td><td>Mounting</td><td>4.1 Stress from mounting head
If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitor and to result in cracking. Please take following precautions.

1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface but do not contact it.
2. Adjust the mounting head pressure to be 1 to 3N of static weight.
3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board. See following examples.
<table>
<tr><th></th><th>Not recommended</th><th>Recommended</th></tr>
<tr><td>Single sided mounting</td><td>Crack</td><td>Support</td></tr>
<tr><td>Double-sides mounting</td><td>Solder peeling
Crack</td><td>Support</td></tr>
</table>
When the centering jaw is worn, mechanical impact on the capacitor may occur and damage the product. Please control the closing dimension of the centering jaw and provide sufficient preventive maintenance and/or replacement if necessary.</td></tr>
</table>

(9. Caution, continued)

No.	Process	Condition
5	Soldering	See below

5.1 Flux selection

Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, the following is recommended.

1. Use a mildly activated rosin flux (less than 0.1wt% chlorine).
2. Excessive flux must be avoided. Please provide proper amount of flux.
3. When water-soluble flux is used, sufficient washing is necessary.

5.2 Recommended soldering profile by various methods

Reflow soldering

Preheating
Soldering
Natural cooling
Peak Temp
Temp. (°C)
ΔT
0
Over 60 sec.
Peak Temp time

Manual soldering
(Solder iron)

300
Temp. (°C)
ΔT
Preheating
0
3sec. (As short as possible)

5.3 Recommended soldering peak temp and duration

Temp./Duration Solder	Reflow soldering	
	Peak temp(°C)	Duration(sec.)
Sn-Pb Solder	230 max.	20 max.
Lead Free Solder	260 max.	10 max.

Recommended solder compositions

Sn-37Pb (Sn-Pb solder)

Sn-3.0Ag-0.5Cu (Lead Free Solder)

(9. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	5.4 Avoiding thermal shock

5.4 Avoiding thermal shock

1. Preheating condition

Soldering	Temp. (°C)
Reflow soldering	∆T ≤ 150
Manual soldering	∆T ≤ 150

2. Cooling condition

   Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (∆T) must be less than 100°C.

5.5 Amount of solder

Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.

Excessive solder	Higher tensile force on the chip capacitor may cause cracking.
Adequate	Maximum amount Minimum amount
Insufficient solder	Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.

5.6 Solder repair by solder iron

1. Selection of the soldering iron tip

   Tip temperatures of solder iron vary by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation; however, heat shock may cause a crack in the chip capacitor. Please make sure the tip temperature before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)

Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)

Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)
300 max.	3 max.	20 max.	Ø 3.0 max.

(9. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	2. Direct contact of the soldering iron with ceramic dielectric of the chip capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron. 5.7 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder. 5.8 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially when the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 “Recommendations to prevent the tombstone phenomenon”.)
6	Cleaning	1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and to deteriorate insulation resistance. 2. If cleaning condition is not suitable, it may deteriorate the chip capacitor. 2.1 Insufficient washing 1. Terminal electrodes may be corroded by Halogen in the flux. 2. Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance. 3. Water soluble flux has higher tendency to have above mentioned problems (1) and (2). 2.2 Excessive washing When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended. Power: 20 W/ℓmax. Frequency: 40 kHz max. Washing time: 5 minutes max. 2.3 If the cleaning fluid is contaminated, concentration of Halogen can increase, and it may bring the same result as insufficient cleaning.

(9. Caution, continued)

No.	Process	Condition
7	Coating and molding of the P.C. Board	1. When the P.C. board is coated, please verify the impact on the capacitor. 2. Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor. 3. Please verify the curing temperature.
8	Handling after chip mounted	1. Please pay attention not to bend or distort the P.C. board after soldering otherwise the chip capacitor may crack. Bend　　Twist 2. When functional check of the P.C. board is performed, high pin pressure tends to be used to avoid poor contact. But if the pressure is excessive and bends the P.C. board, it may crack the chip capacitor or peel the termination. Please adjust the check pins accordingly to ensure the P.C. board is not flexed.

Item	Not recommended	Recommended
Board bending	Termination peeling Check pin	Support pin Check pin

(9. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitors	1. The chip capacitor may crack if dropped, especially large case sizes. Please handle with care and do not use if dropped. Crack Floor 2. When stacking the P.C. board for storage or handling after soldering, the corner of the P.C. board may hit the chip capacitor of a neighboring board to cause a crack. P.C. Board Crack
10	Capacitance aging	Class 2 capacitors have an aging characteristic, which is a decrease in capacitance over time due to crystalline changes that occur I ferroelectric ceramics. Careful consideration should be done in case of the time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life and (failure rate) depend on the temperature and voltage applied. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 "Calculation of the estimated lifetime and the failure rate." The risk can be decreased by reducing the temperature and the voltage but the failure rate can not be guaranteed.
12	Others	The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition. The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet: Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, ships, etc.) Medical equipment. Power-generation control equipment. Atomic energy-related equipment. Seabed equipment. Transportation control equipment. Public information-processing equipment. Military equipment. Electric heating apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose applications. When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup circuits, etc., to ensure higher safety.

10. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

1) Inspection No.
2) TDK P/N
3) Customer's P/N
4) Quantity

*Composition of Inspection No.

Example	M	0	A	–	OO	–	OOO
	(a)	(b)	(c)		(d)		(e)

a) Line code
b) Last digit of the year
c) Month and A for January and B for February and so on. (Skip I)
d) Inspection Date of the month.
e) Serial No. of the day

11. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

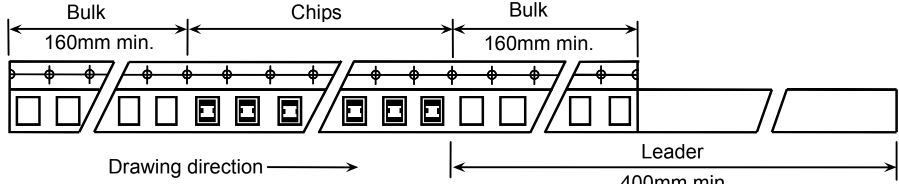
12. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1. Dimensions of carrier tape

   Dimensions of paper tape shall be according to Appendix 7, 8.
   Dimensions of plastic tape shall be according to Appendix 9

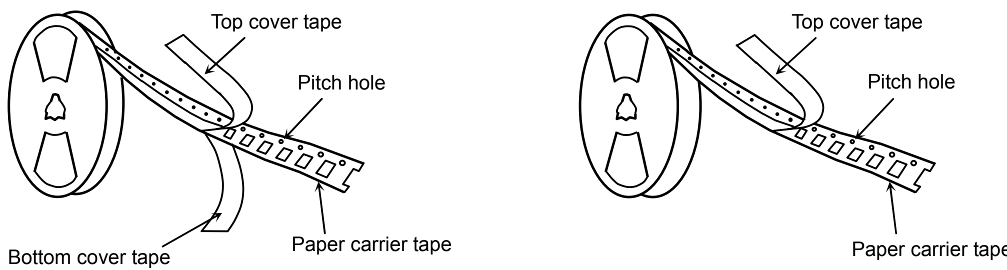
2. Bulk part and leader of taping



3. Dimensions of reel

   Dimensions of Ø178 reel shall be according to Appendix 10
   Dimensions of Ø330 reel shall be according to Appendix 11.

4. Structure of taping



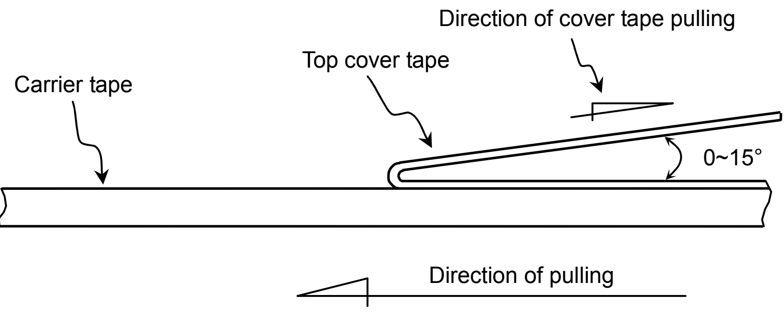
2. CHIP QUANTITY

Type	Thickness of chip	Taping Material	Chip quantity (pcs.)	
			φ178mm reel	φ330mm reel
CKD710JB	0.30 mm	Paper	10,000	50,000
CKD610JB	0.80 mm	Paper	4,000	10,000
CKD510JB	0.85 mm	Paper	4,000	10,000
CKD110JB	0.85 mm	Paper	4,000	10,000
CKD310JB	1.60mm MAX.	Plastic	2,000	10,000

3. PERFORMANCE SPECIFICATIONS

3-1. Peel back cover (top tape)

0.05-0.7N. (See the following figure.)



3-2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

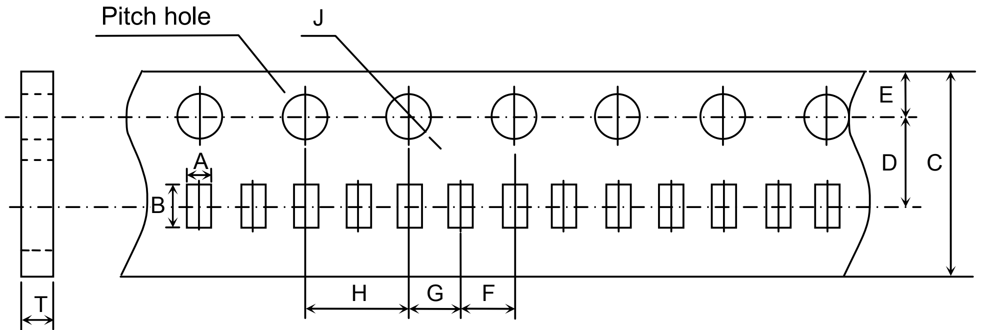
3-3. The missing of components shall be less than 0.1%

3-4. Components shall not stick to the cover tape.

3-5. The cover tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 7

Paper Tape



(Unit : mm)

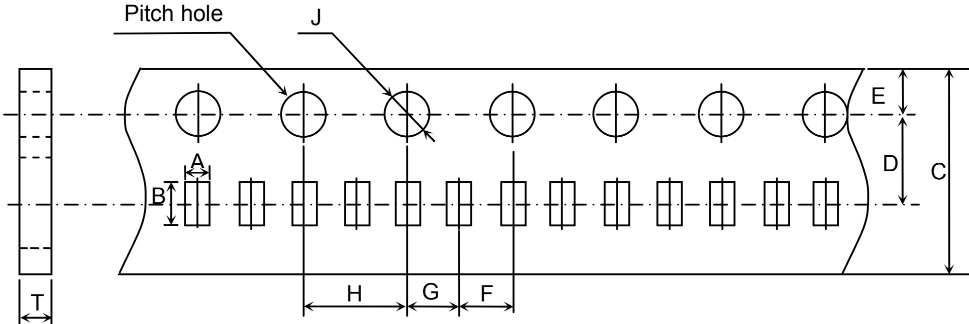
Symbol / Type	A	B	C	D	E	F
CKD710JB	(0.65)	(1.15)	8.00±0.30	3.50±0.05	1.75±0.10	2.00±0.05

Symbol / Type	G	H	J	T
CKD710JB	2.00±0.05	4.00±0.10	Ø 1.5 $^{+0.10}_{0}$	0.60±0.05

* The values in the parentheses ( ) are for reference.

Appendix 8

Paper Tape



(Unit: mm)

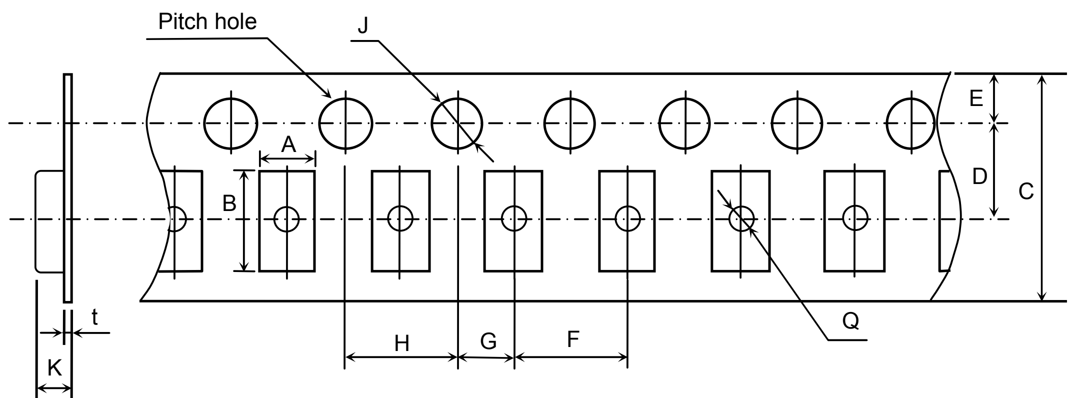
Symbol / Type	A	B	C	D	E	F
CKD610JB	(1.10)	(1.90)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10
CKD510JB	(1.50)	(2.30)				
CKD110JB	(1.65)	(3.50)				

Symbol / Type	G	H	J	T
CKD610JB	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 $^{+0.10}_{0}$	1.10 max.
CKD510JB				
CKD110JB				

* The values in the parentheses ( ) are for reference.

Appendix 9

Plastic Tape



(Unit: mm)

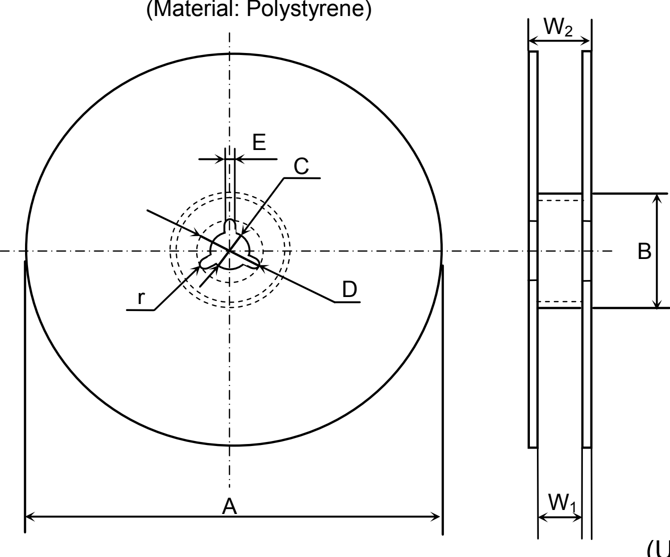
Symbol / Type	A	B	C	D	E	F
CKD310JB	(1.90)	(3.50)	8.00 ± 0.30	3.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10

Symbol / Type	G	H	J	K	t	Q
CKD310JB	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 $^{+0.10}_{0}$	2.50 max.	0.30 max.	Ø 0.50 min.

* The values in the parentheses (   ) are for reference.

Appendix 10

(Material: Polystyrene)



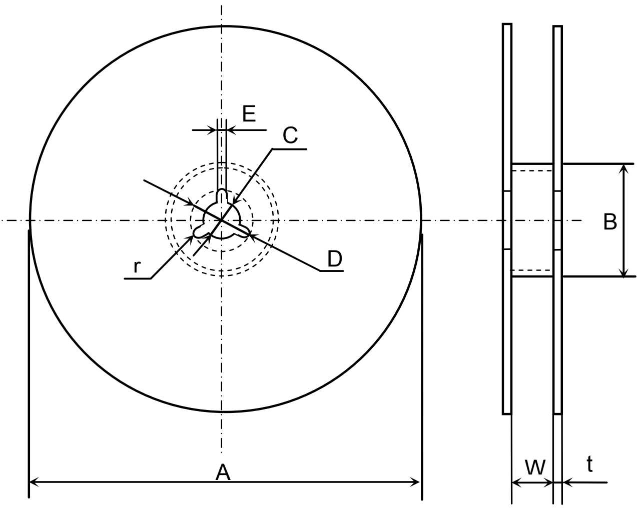
(Unit: mm)

Symbol	A	B	C	D	E	W_1
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	9.0 ± 0.3

Symbol	W_2	r
Dimension	13.0 ± 1.4	1.0

Appendix 11

(Material: Polystyrene)



(Unit: mm)

Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	10.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0

END PAGE