



# SPECIFICATION

SPEC. No. \_\_\_\_\_

DATE : \_\_\_\_\_

Customer  
\_\_\_\_\_

CUSTOMER'S PRODUCT NAME

TDK PRODUCT NAME  
MULTILAYER CERAMIC CHIP CAPACITORS  
C0603 Type / 25V  
COG Characteristics High Q Capacitors

Please sign and return this specification to TDK representatives. If orders are placed without this returned documentation, we must consider you found the specification acceptable.

## THIS SPECIFICATION IS RECEIVED

DATE: \_\_\_\_\_ YEAR \_\_\_\_\_ MONTH \_\_\_\_\_ DAY \_\_\_\_\_

TDK-EPC Corporation  
1-13-1, Nihonbashi, Chuo-ku, Tokyo  
103-0027, Japan

### ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office \_\_\_\_\_

Sales Tel. \_\_\_\_\_ ( ) \_\_\_\_\_

PRODUCT CLASSIFICATION  
CODE

040320

## 1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over the other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd, TDK-EPC HONG KONG LIMITED, TDK (Malaysia) Sdn. Bhd, and TDK Components U.S.A. Inc.

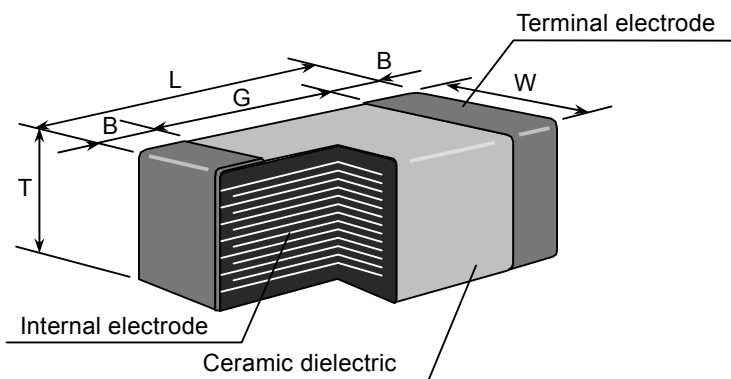
### EXPLANATORY NOTE:

This specification warrants the quality of the ceramic chip capacitors. The product should be evaluated and confirmed a state of mounted on your product before use. If the use of the product exceeds the bounds of this specification, we can not guarantee its quality and reliability.

## 2. CODE CONSTRUCTION

(Example)     C0603     C0G     1E     150     J     T  
                   (1)           (2)           (3)           (4)           (5)           (6)

### 1. Type



Please refer to product list for the dimension of each product. See Section 9 for inside structure and material.

### 2. Temperature Characteristics (Details are shown in Section 7, No.6 )

### 3. Rated Voltage

Symbol	Rated Voltage
1 E	DC 25 V

### 4. Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and second digits identify the first and second significant figures of the capacitance; the third digit identifies the multiplier.

R is designated for a decimal point.

Example 150 → 15pF

5. Capacitance tolerance

Symbol	Tolerance	Capacitance
B	± 0.1 pF	10pF and under
C	± 0.25 pF	
D	± 0.5 pF	
E	± 0.2 pF	
G	± 2 %	Over 10pF
J	± 5 %	

6. Packaging

Symbol	Packaging
T	Taping

**3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE**

1. Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance		Rated capacitance
1	C0G	10pF and under	B (± 0.10 pF)	0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9
			C (± 0.25 pF)	1.0, 1.2, 1.5, 1.8, 2.0, 2.2, 2.7, 3.0
		D (± 0.50 pF)	3.3, 3.9, 4.0, 4.7, 5.0, 5.6, 6.0, 6.8	
		E (± 0.20 pF)	7.0, 8.0, 8.2, 9.0	
		Over 10pF	G (± 2 %)	10.0
			J (± 5 %)	E – 24 series

2. Capacitance Step in E series

E series	Capacitance Step		
E- 3	1.0	2.2	4.7

**4. OPERATING TEMPERATURE RANGE**

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
C0G	-55°C	125°C	25°C

**5. STORING CONDITION AND TERM**

5 to 40°C at 20 to 70%RH  
6 months Max.

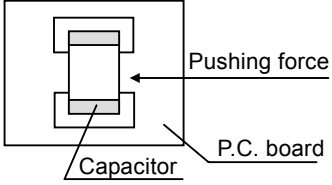
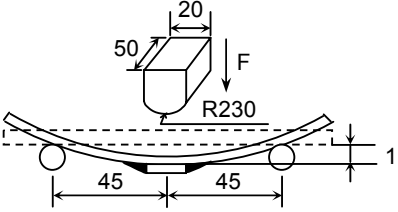
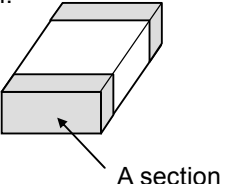
**6. INDUSTRIAL WASTE DISPOSAL**

Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

## 7. PERFORMANCE

No.	Item	Performance	Test or inspection method						
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass (10X)						
2	Insulation Resistance	10,000MΩ min.	Apply rated voltage for 60s.						
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	<table border="1"> <thead> <tr> <th>Class</th> <th>Apply voltage</th> </tr> </thead> <tbody> <tr> <td>Class1</td> <td>3 × rated voltage</td> </tr> </tbody> </table> <p>Above DC voltage shall be applied for 1 to 5s. Charge / discharge current shall not exceed 50mA.</p>	Class	Apply voltage	Class1	3 × rated voltage		
Class	Apply voltage								
Class1	3 × rated voltage								
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Class</th> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>Class1</td> <td>1MHz±10%</td> <td>0.5 - 5 Vrms.</td> </tr> </tbody> </table>	Class	Measuring frequency	Measuring voltage	Class1	1MHz±10%	0.5 - 5 Vrms.
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Class1	1MHz±10%	0.5 - 5 Vrms.							
5	Q (Class 1)	<table border="1"> <thead> <tr> <th>Rated Capacitance</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>30pF and over</td> <td>1,000 min.</td> </tr> <tr> <td>Under 30pF</td> <td>400+20×C min.</td> </tr> </tbody> </table> <p>C : Rated capacitance (pF)</p>	Rated Capacitance	Q	30pF and over	1,000 min.	Under 30pF	400+20×C min.	See No.4 in this table for measuring condition.
Rated Capacitance	Q								
30pF and over	1,000 min.								
Under 30pF	400+20×C min.								
6	Temperature Characteristics of Capacitance (Class 1)	<table border="1"> <thead> <tr> <th>T.C.</th> <th>Temperature Coefficient (ppm/°C)</th> </tr> </thead> <tbody> <tr> <td>C0G</td> <td>0 ± 30</td> </tr> </tbody> </table> <p>Capacitance drift: Within ± 0.2% or ±0.05pF, whichever larger.</p>	T.C.	Temperature Coefficient (ppm/°C)	C0G	0 ± 30	<p>Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature.</p> <p>Measuring temperature below 20°C shall be -10°C and -25°C.</p>		
T.C.	Temperature Coefficient (ppm/°C)								
C0G	0 ± 30								

(7. Performance, continued)

No.	Item	Performance	Test or inspection method
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	Reflow solder the capacitor on P.C. board (shown in Appendix 1) and apply a pushing force of 2N with 10±1s. 
8	Bending	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 2) and bends 1mm.  <p style="text-align: right;">(Unit: mm)</p>
9	Solderability	New solder to cover over 75% of termination. 25% may have pin holes or rough spots but not concentrated in one spot. Ceramic surface of "A sections" shall not be exposed due to melting or shifting of termination material. 	Completely soak both terminations in solder at 235±5°C for 2±0.5s. Solder : H63A (JIS Z 3282) Flux : Isopropyl alcohol (JIS K 8839) Rosin(JIS K 5902) 25% solid solution.

(7. Performance, continued)

No.	Item		Performance	Test or inspection method							
10	Resistance to solder heat	External appearance	No cracks are allowed and terminations shall be covered at least 60% with new solder.	Completely soak both terminations in solder at 260±5°C for 5±1s.  Preheating condition Temp. : 150±10°C Time : 1 to 2min.  Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.  Solder : H63A (JIS Z 3282)  Leave the capacitor in ambient conditions for 6 to 24h before measurement.							
		Capacitance	<table border="1"> <tr> <td colspan="2">Characteristics</td> <td>Change from the value before test</td> </tr> <tr> <td>Class 1</td> <td>C0G</td> <td>±2.5% or ±0.25pF, whichever larger.</td> </tr> </table>		Characteristics		Change from the value before test	Class 1	C0G	±2.5% or ±0.25pF, whichever larger.	
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			Rated Capacitance		Q						
30pF and over	1,000 min.										
Under 30pF	400+20×C min.										
Insulation Resistance	Meet the initial spec.										
Voltage proof	No insulation breakdown or other damage.										
11	Vibration	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.  Vibrate the capacitors with amplitude of 1.5mm P-P changing the frequencies from 10Hz to 55Hz and back to 10Hz in about 1min. Repeat this for 2h each in 3 perpendicular directions.							
		Capacitance	<table border="1"> <tr> <td colspan="2">Characteristics</td> <td>Change from the value before test</td> </tr> <tr> <td>Class 1</td> <td>C0G</td> <td>±2.5% or ±0.25pF, whichever larger.</td> </tr> </table>		Characteristics		Change from the value before test	Class 1	C0G	±2.5% or ±0.25pF, whichever larger.	
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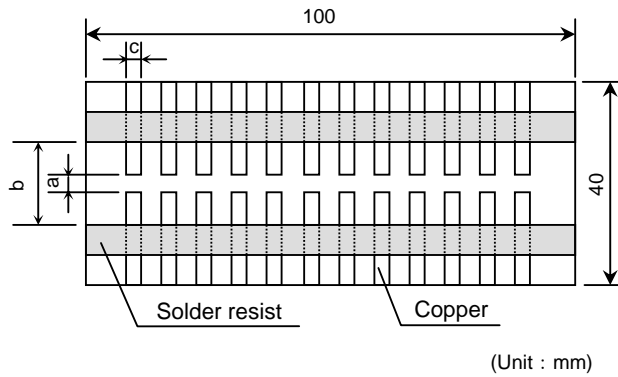
## (7. Performance, continued)

No.	Item		Performance	Test or inspection method															
12	Temperature cycle	External appearance	No mechanical damage.	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.</p> <p>Expose the capacitor in the conditions step1 through step 4 and repeat 5 times consecutively.</p> <p>Leave the capacitor in ambient conditions for 6 to 24h before measurement.</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time (min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>-55 ±3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>Reference Temp.</td> <td>2 - 5</td> </tr> <tr> <td>3</td> <td>125 ± 2</td> <td>30 ± 2</td> </tr> <tr> <td>4</td> <td>Reference Temp.</td> <td>2 - 5</td> </tr> </tbody> </table>	Step	Temperature(°C)	Time (min.)	1	-55 ±3	30 ± 3	2	Reference Temp.	2 - 5	3	125 ± 2	30 ± 2	4	Reference Temp.	2 - 5
		Step	Temperature(°C)		Time (min.)														
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30pF and over	1,000 min.																		
Under 30pF	400+20×C min.																		
Insulation Resistance	Meet the initial spec.																		
Voltage proof	No insulation breakdown or other damage.																		
13	Moisture Resistance (Steady State)	External appearance	No mechanical damage.	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.</p> <p>Leave at temperature 40±2°C, 90 to 95%RH for 500 +24,0h.</p> <p>Leave the capacitor in ambient conditions for 6 to 24h before measurement.</p>															
		Capacitance	<table border="1"> <thead> <tr> <th colspan="2">Characteristics</th> <th>Change from the value before test</th> </tr> </thead> <tbody> <tr> <td>Class 1</td> <td>C0G</td> <td>±5% or ±0.5pF, whichever larger.</td> </tr> </tbody> </table>		Characteristics		Change from the value before test	Class 1	C0G	±5% or ±0.5pF, whichever larger.									
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Under 10pF	200+10×C min.																		
Insulation Resistance	1,000MΩ min.																		

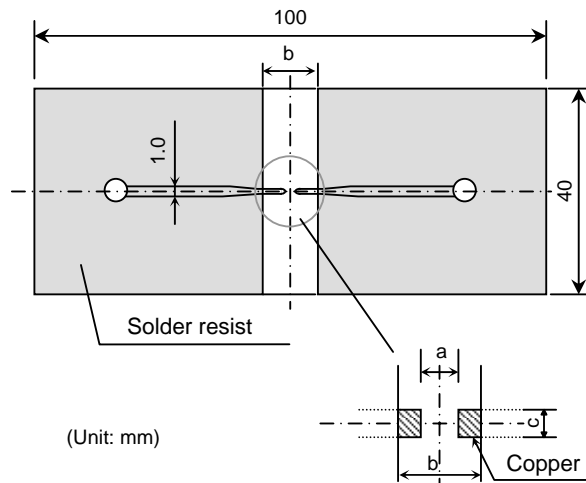
(7. Performance, continued)

No.	Item		Performance	Test or inspection method					
14	Moisture Resistance	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.  Apply the rated voltage at temperature $40\pm 2^{\circ}\text{C}$ and 90 to 95%RH for 500 +24,0h.  Charge/discharge current shall not exceed 50mA.  Leave the capacitor in ambient conditions for 6 to 24h before measurement.					
		Capacitance	<table border="1" data-bbox="581 348 948 533"> <thead> <tr> <th colspan="2" data-bbox="581 348 760 380">Characteristics</th> <th data-bbox="760 348 948 380">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 453 672 485">Class 1</td> <td data-bbox="672 453 760 485">COG</td> <td data-bbox="760 422 948 533"><math>\pm 7.5\%</math> or <math>\pm 0.75\text{pF}</math>, whichever larger.</td> </tr> </tbody> </table>		Characteristics		Change from the value before test	Class 1	COG
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	Class 1	COG	$\pm 7.5\%$ or $\pm 0.75\text{pF}$ , whichever larger.						
Q (Class 1)	<table border="1" data-bbox="581 606 948 726"> <thead> <tr> <th data-bbox="581 606 769 638">Rated Capacitance</th> <th data-bbox="769 606 948 638">Q</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 638 769 690">30pF and over</td> <td data-bbox="769 638 948 690">200 min.</td> </tr> <tr> <td data-bbox="581 690 769 726">Under 30pF</td> <td data-bbox="769 690 948 726"><math>100 + 10/3 \times C</math> min.</td> </tr> </tbody> </table> <p data-bbox="711 737 959 764" style="text-align: center;">C : Rated capacitance (pF)</p>	Rated Capacitance	Q	30pF and over	200 min.	Under 30pF	$100 + 10/3 \times C$ min.		
Rated Capacitance	Q								
30pF and over	200 min.								
Under 30pF	$100 + 10/3 \times C$ min.								
Insulation Resistance	500M $\Omega$ min.								
17	Life	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.  Apply $2 \times$ rated voltage at $125 \pm 2^{\circ}\text{C}$ for 1,000 +48,0h  Charge/discharge current shall not exceed 50mA.  Leave the capacitor in ambient conditions for 6 to 24h before measurement.					
		Capacitance	<table border="1" data-bbox="581 1031 948 1184"> <thead> <tr> <th colspan="2" data-bbox="581 1031 760 1062">Characteristics</th> <th data-bbox="760 1031 948 1062">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 1115 672 1146">Class 1</td> <td data-bbox="672 1115 760 1146">COG</td> <td data-bbox="760 1083 948 1184"><math>\pm 3\%</math> or <math>\pm 0.3\text{pF}</math>, whichever larger.</td> </tr> </tbody> </table>		Characteristics		Change from the value before test	Class 1	COG
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	Class 1	COG	$\pm 3\%$ or $\pm 0.3\text{pF}$ , whichever larger.						
Q (Class 1)	<table border="1" data-bbox="581 1262 948 1436"> <thead> <tr> <th data-bbox="581 1262 769 1293">Rated Capacitance</th> <th data-bbox="769 1262 948 1293">Q</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 1293 769 1346">30pF and over</td> <td data-bbox="769 1293 948 1346">350 min.</td> </tr> <tr> <td data-bbox="581 1346 769 1398">10pF and over under 30pF</td> <td data-bbox="769 1346 948 1398"><math>275 + 5/2 \times C</math> min.</td> </tr> <tr> <td data-bbox="581 1398 769 1436">Under 10pF</td> <td data-bbox="769 1398 948 1436"><math>200 + 10 \times C</math> min.</td> </tr> </tbody> </table> <p data-bbox="711 1446 959 1474" style="text-align: center;">C : Rated capacitance (pF)</p>	Rated Capacitance	Q	30pF and over	350 min.	10pF and over under 30pF	$275 + 5/2 \times C$ min.	Under 10pF	$200 + 10 \times C$ min.
Rated Capacitance	Q								
30pF and over	350 min.								
10pF and over under 30pF	$275 + 5/2 \times C$ min.								
Under 10pF	$200 + 10 \times C$ min.								
Insulation Resistance	1,000M $\Omega$ min.								

**Appendix - 1**  
**P.C. Board for reliability test**



**Appendix - 2**  
**P.C. Board for bending test**



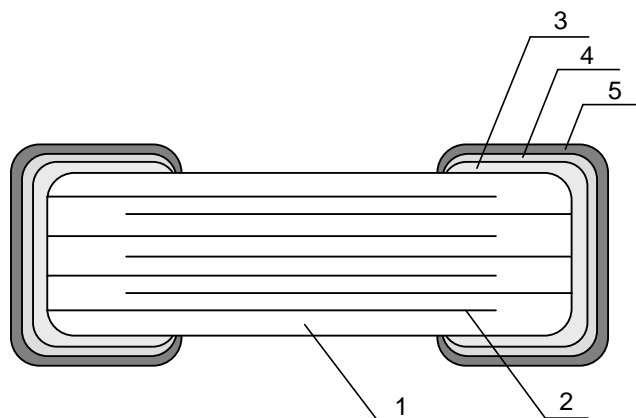
Material: Glass Epoxy (As per JIS C6484 GE4)

P.C. Board thickness: Appendix-2    0.8mm  
Appendix-1    1.6mm

TDK (EIA style)	Dimensions (mm)		
	a	b	c
C0603 (CC0201)	0.3	0.8	0.3

- Copper (thickness 0.035mm)
- Solder resist

## 8. INSIDE STRUCTURE AND MATERIAL

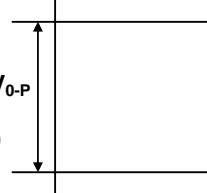
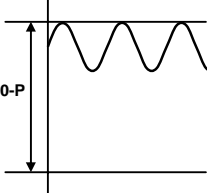
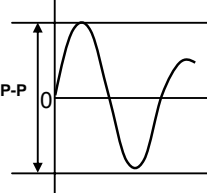
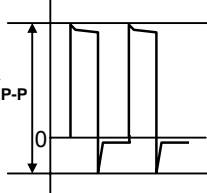
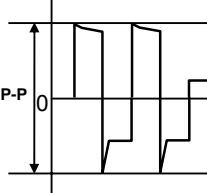
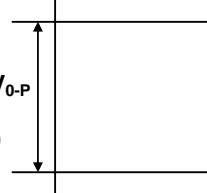
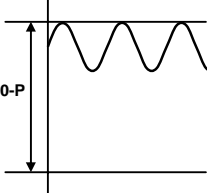
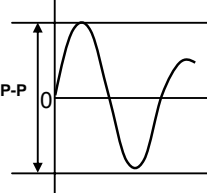
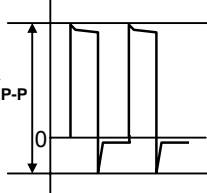
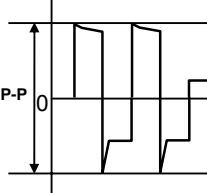
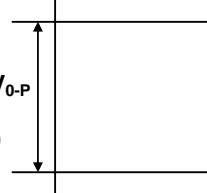
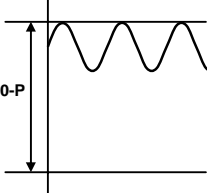
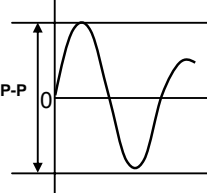
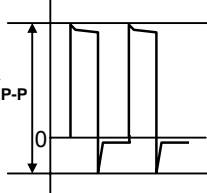
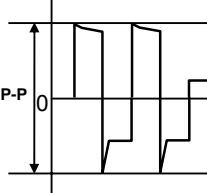


No.	NAME	MATERIAL
1	Dielectric	CaZrO <sub>3</sub>
2	Electrode	Nickel (Ni)
3	Termination	Copper (Cu)
4		Nickel (Ni)
5		Tin (Sn)

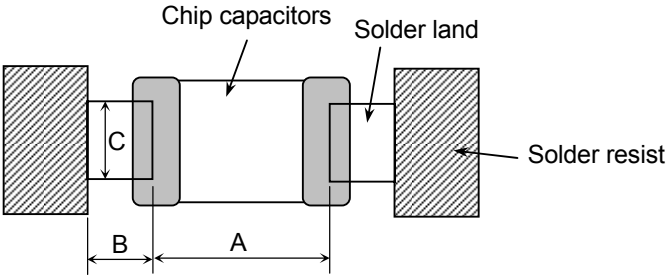
## 9. SOLDERING CONDITION

As for C0603 type, reflow soldering only.

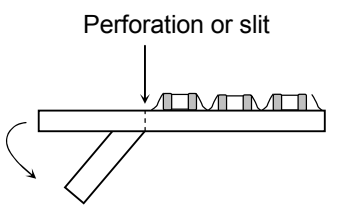
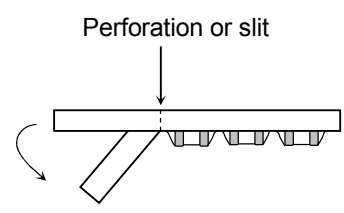
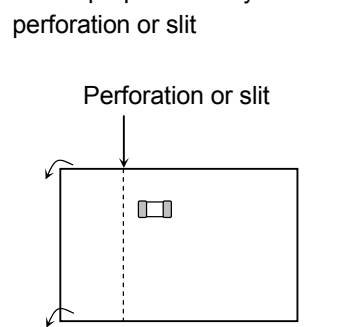
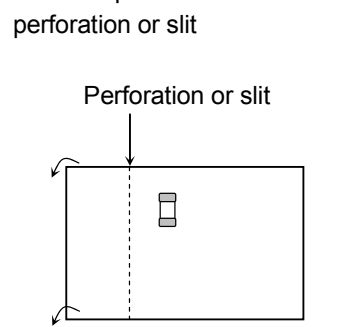
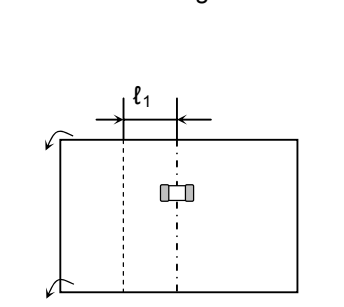
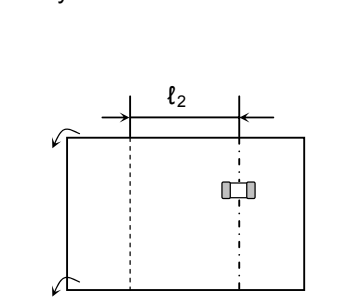
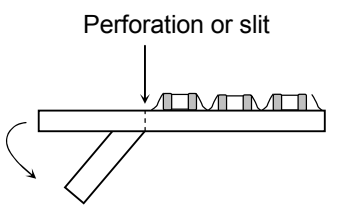
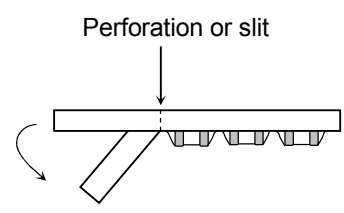
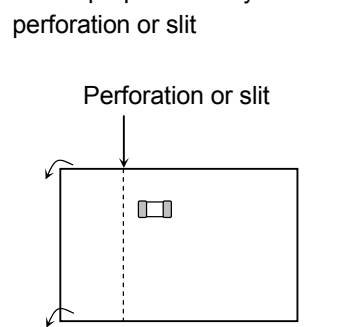
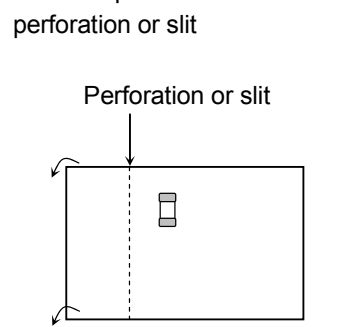
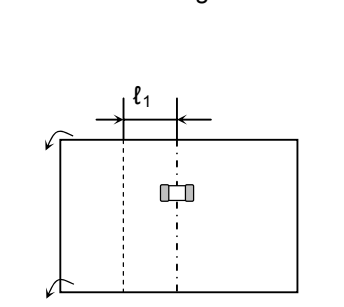
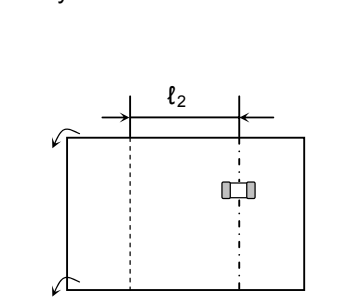
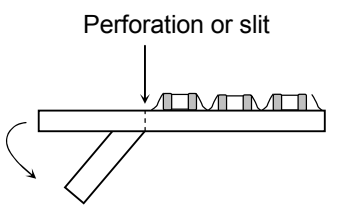
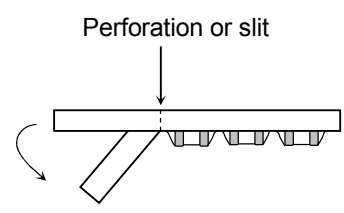
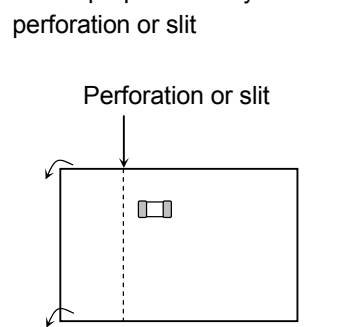
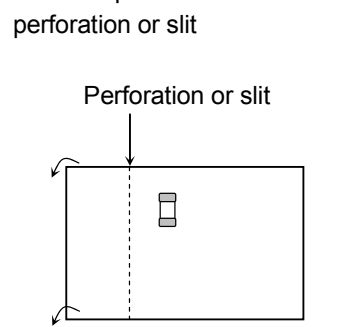
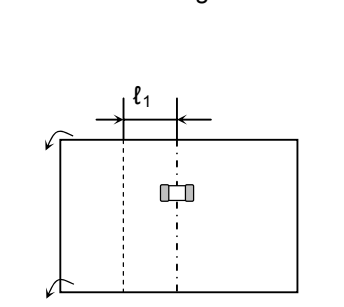
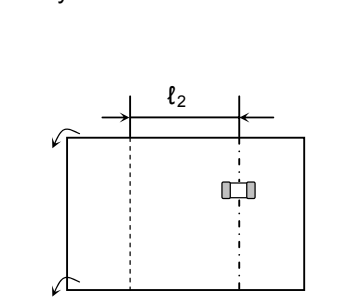
## 10. Caution

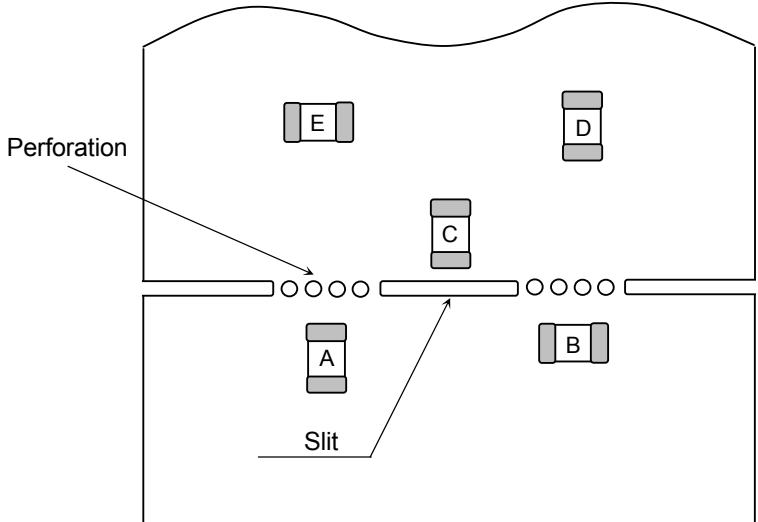
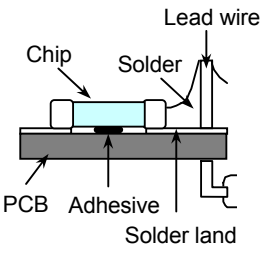
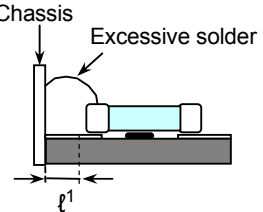
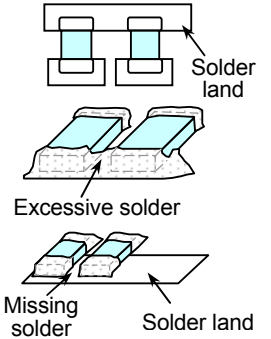
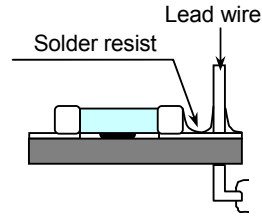
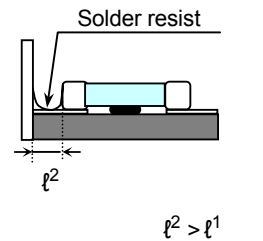
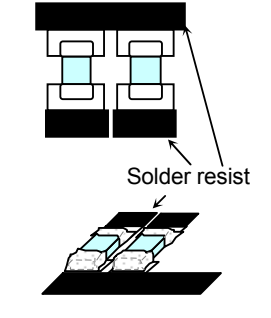
No.	Process	Condition																
1	Operating Condition (Storage, Transportation)	<p>1.1 Storage</p> <ol style="list-style-type: none"> <li>The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt.</li> <li>The capacitor must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur.</li> <li>Avoid storing in sun light and falling of dew.</li> <li>Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability.</li> <li>Capacitor should be tested for solderability when stored for long periods of time.</li> </ol> <p>1.2 Handling in transportation</p> <p>In case of the transportation, the performance of the capacitor may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 "Handling in Transportation")</p>																
2	Circuit design	<p>2.1 Operating temperature</p> <p>Operating temperature should be followed strictly within this specification.</p> <ol style="list-style-type: none"> <li>Do not use capacitors above the maximum allowable operating temperature.</li> <li>Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product it's mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C)</li> <li>The electrical characteristics of the capacitor will vary depending on the temperature. The capacitor should be selected and designed after taking temperature into consideration.</li> </ol> <p>2.2 Operating voltage</p> <ol style="list-style-type: none"> <li>Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, <math>V_{0-P}</math> must be below the rated voltage. Reference figures 1 and 2 below. AC or pulse with overshooting, <math>V_{P-P}</math> must be below the rated voltage. Reference figures 3, 4, and 5 below. When the voltage is started/stopped to apply to the circuit an irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within its rated voltage during these Irregular voltage periods.</li> </ol> <table border="1" data-bbox="505 1312 1414 1843"> <thead> <tr> <th data-bbox="505 1312 683 1354">Voltage</th> <th data-bbox="683 1312 927 1354">(1) DC voltage</th> <th data-bbox="927 1312 1170 1354">(2) DC+AC voltage</th> <th data-bbox="1170 1312 1414 1354">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="505 1354 683 1570">Positional Measurement (Rated voltage)</td> <td data-bbox="683 1354 927 1570">  </td> <td data-bbox="927 1354 1170 1570">  </td> <td data-bbox="1170 1354 1414 1570">  </td> </tr> <tr> <th data-bbox="505 1591 683 1633">Voltage</th> <th data-bbox="683 1591 927 1633">(4) Pulse voltage (A)</th> <th data-bbox="927 1591 1170 1633">(5) Pulse voltage (B)</th> <th></th> </tr> <tr> <td data-bbox="505 1633 683 1843">Positional Measurement (Rated voltage)</td> <td data-bbox="683 1633 927 1843">  </td> <td data-bbox="927 1633 1170 1843">  </td> <td></td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)		Positional Measurement (Rated voltage)			
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(10. Caution, continued)

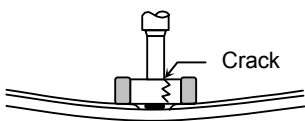
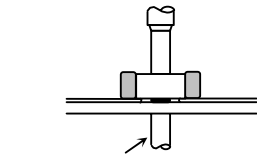
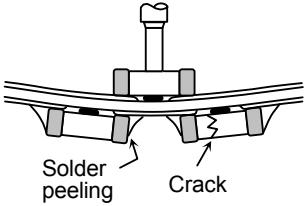
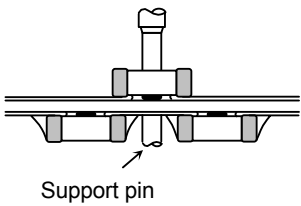
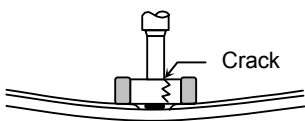
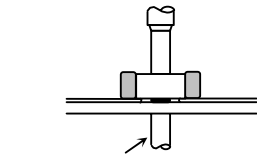
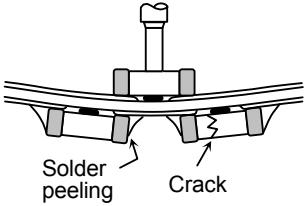
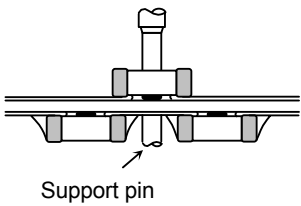
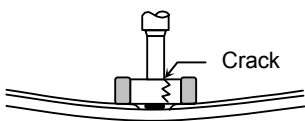
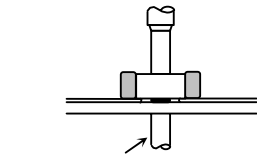
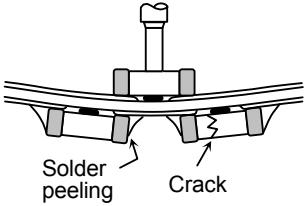
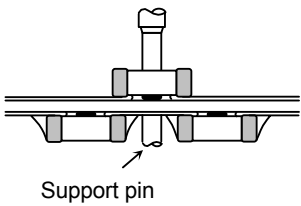
No.	Process	Condition															
2	Circuit design (continued)	<p>2.2 Operating Voltage (continued)</p> <p>2. Even below the rated voltage, if repetitive high AC frequency or pulsed voltage is applied, the reliability of the capacitors may be reduced.</p> <p>3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitor should be selected after considering the voltage affects.</p> <p>2.3 Frequency</p> <p>When Class 2 capacitors are used in AC and/or pulsed voltages, the capacitor may self vibrate and generate audible sound (piezoelectric affect).</p>															
3	Designing P.C. Board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitor.</p> <p>1. The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.</p> <p>2. Avoid using common solder land for multiple terminations and provide individual solder land for each termination instead.</p> <p>3. Size and recommended land dimensions provided below:</p> <div style="text-align: center;">  </div> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2" style="text-align: left;">Reflow soldering</th> <th style="text-align: right;">(mm)</th> </tr> <tr> <th style="text-align: left;">Symbol \ Type</th> <th colspan="2" style="text-align: center;">C0603 [CC0201]</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">A</td> <td colspan="2" style="text-align: center;">0.25 - 0.35</td> </tr> <tr> <td style="text-align: center;">B</td> <td colspan="2" style="text-align: center;">0.2 - 0.3</td> </tr> <tr> <td style="text-align: center;">C</td> <td colspan="2" style="text-align: center;">0.25 - 0.35</td> </tr> </tbody> </table>	Reflow soldering		(mm)	Symbol \ Type	C0603 [CC0201]		A	0.25 - 0.35		B	0.2 - 0.3		C	0.25 - 0.35	
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(10. Caution, continued)

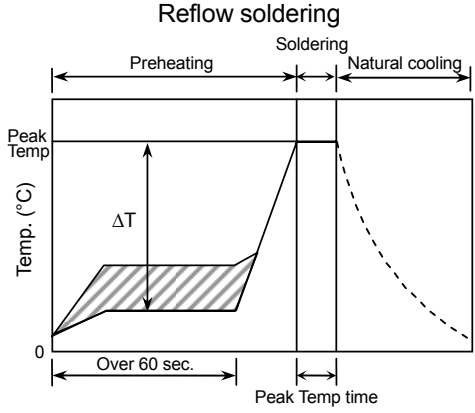
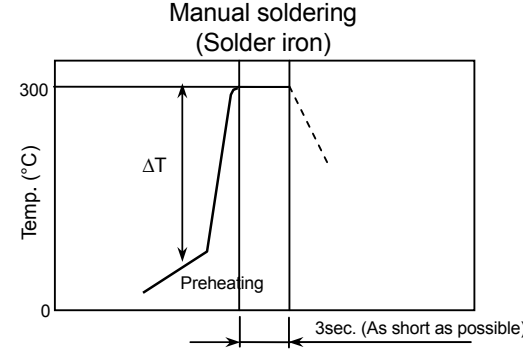
No.	Process	Condition												
3	Designing P.C. Board (continued)	<p>4. Recommended chip capacitor layout is as following provided below:</p> <table border="1"> <thead> <tr> <th data-bbox="506 235 683 310"></th> <th data-bbox="683 235 1040 310">Disadvantage against bending stress</th> <th data-bbox="1040 235 1398 310">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="506 310 683 701">Mounting face</td> <td data-bbox="683 310 1040 701"> <p>Perforation or slit</p>  <p>Break P.C.board with mounted side up.</p> </td> <td data-bbox="1040 310 1398 701"> <p>Perforation or slit</p>  <p>Break P.C.board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="506 701 683 1121">Chip arrangement (Direction)</td> <td data-bbox="683 701 1040 1121"> <p>Mount perpendicularly to perforation or slit</p>  </td> <td data-bbox="1040 701 1398 1121"> <p>Mount in parallel with perforation or slit</p>  </td> </tr> <tr> <td data-bbox="506 1121 683 1570">Distance from slit</td> <td data-bbox="683 1121 1040 1570"> <p>Closer to slit is higher stress</p>  <p><math>(l_1 &lt; l_2)</math></p> </td> <td data-bbox="1040 1121 1398 1570"> <p>Away from slit is less stress</p>  <p><math>(l_1 &lt; l_2)</math></p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p>Perforation or slit</p>  <p>Break P.C.board with mounted side up.</p>	<p>Perforation or slit</p>  <p>Break P.C.board with mounted side down.</p>	Chip arrangement (Direction)	<p>Mount perpendicularly to perforation or slit</p> 	<p>Mount in parallel with perforation or slit</p> 	Distance from slit	<p>Closer to slit is higher stress</p>  <p><math>(l_1 &lt; l_2)</math></p>	<p>Away from slit is less stress</p>  <p><math>(l_1 &lt; l_2)</math></p>
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No.	Process	Condition	
3	Designing P.C. board (continued)	<p>5. Mechanical stress varies according to location of chip capacitor on the P.C.board.</p>  <p>The relative stress applied to these capacitors during depaneling in the following order.</p> $A > B = C > D > E$	
6. Layout recommendation			
Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid			
Recommendation			

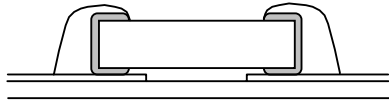
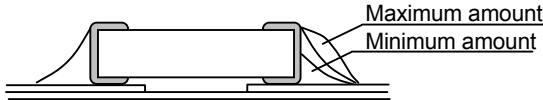
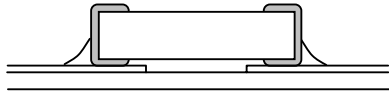
(10. Caution, continued)

No.	Process	Condition									
4	Mounting	<p>4.1 Stress from mounting head</p> <p>If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitor and result in cracking. Please take following precautions:</p> <ol style="list-style-type: none"> <li>1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface but not contact it</li> <li>2. Adjust the mounting head pressure to be 1 to 3N of static weight.</li> <li>3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board.</li> </ol> <p>See following examples.</p> <table border="1" data-bbox="516 558 1403 1087"> <thead> <tr> <th data-bbox="516 558 695 611"></th> <th data-bbox="695 558 1057 611">Not recommended</th> <th data-bbox="1057 558 1403 611">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="516 611 695 842">Single sided mounting</td> <td data-bbox="695 611 1057 842">  </td> <td data-bbox="1057 611 1403 842">  </td> </tr> <tr> <td data-bbox="516 842 695 1087">Double-sided mounting</td> <td data-bbox="695 842 1057 1087">  </td> <td data-bbox="1057 842 1403 1087">  </td> </tr> </tbody> </table> <p>When the centering jaw is worn, mechanical impact on the capacitor may occur and damage the product. Please control the closing dimension of the centering jaw and provide sufficient preventive maintenance and/or replacement of it.</p>		Not recommended	Recommended	Single sided mounting			Double-sided mounting		
	Not recommended	Recommended									
Single sided mounting											
Double-sided mounting											

(10. Caution, continued)

No.	Process	Condition														
5	Soldering (continued)	<p>5.1 Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, it is recommended following.</p> <ol style="list-style-type: none"> <li>1. It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine).</li> <li>2. Excessive flux must be avoided. Please provide proper amount of flux.</li> <li>3. When water-soluble flux is used, sufficient washing is necessary.</li> </ol> <p>5.2 Recommended soldering profile by various methods</p> <div style="text-align: center;"> <p><b>Reflow soldering</b></p>  </div> <div style="text-align: center; margin-top: 20px;"> <p><b>Manual soldering (Solder iron)</b></p>  </div> <p>5.3 Recommended soldering peak temp and duration</p> <table border="1" data-bbox="548 1417 1096 1638"> <thead> <tr> <th rowspan="2" style="text-align: center;">Temp./Duration</th> <th colspan="2" style="text-align: center;">Reflow soldering</th> </tr> <tr> <th style="text-align: center;">Peak temp(°C)</th> <th style="text-align: center;">Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Solder</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">Sn-Pb Solder</td> <td style="text-align: center;">230 max.</td> <td style="text-align: center;">20 max.</td> </tr> <tr> <td style="text-align: center;">Lead Free Solder</td> <td style="text-align: center;">260 max.</td> <td style="text-align: center;">10 max.</td> </tr> </tbody> </table> <p>Recommended solder compositions                      Sn-37Pb (Sn-Pb solder)                      Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>	Temp./Duration	Reflow soldering		Peak temp(°C)	Duration(sec.)	Solder			Sn-Pb Solder	230 max.	20 max.	Lead Free Solder	260 max.	10 max.
Temp./Duration	Reflow soldering															
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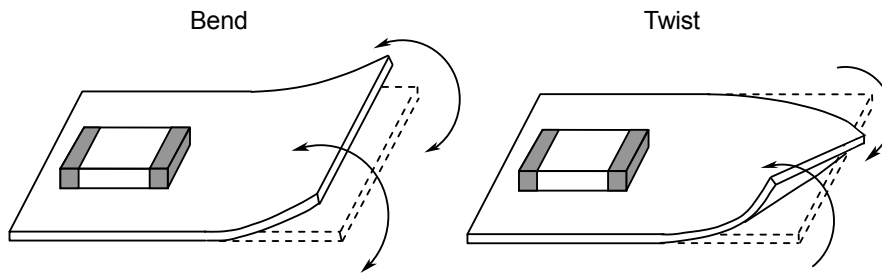
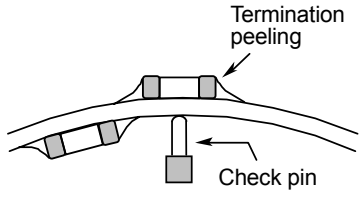
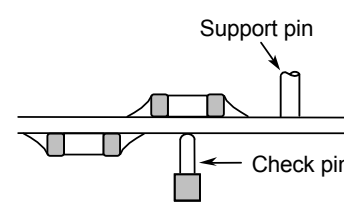
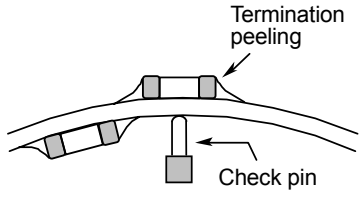
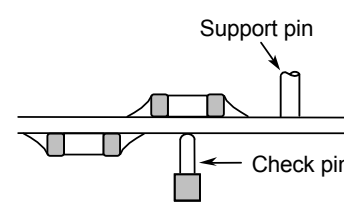
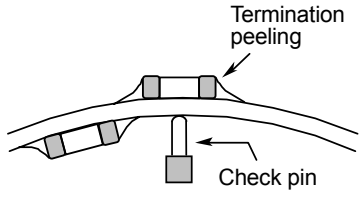
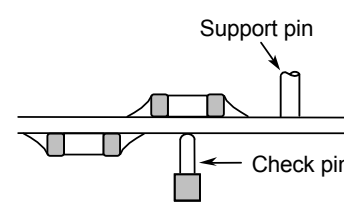
(10. Caution, continued)

No.	Process	Condition																	
5	Soldering (continued)	<p data-bbox="488 180 786 210">5.4 Avoiding thermal shock</p> <p data-bbox="488 218 756 247">1. Preheating condition</p> <table border="1" data-bbox="581 247 1261 401"> <thead> <tr> <th data-bbox="581 258 808 296">Soldering</th> <th data-bbox="808 258 1036 296">Type</th> <th data-bbox="1036 258 1261 296">Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 306 808 344">Reflow soldering</td> <td data-bbox="808 306 1036 344">C0603(CC0201)</td> <td data-bbox="1036 306 1261 344"><math>\Delta T \leq 150</math></td> </tr> <tr> <td data-bbox="581 354 808 392">Manual soldering</td> <td data-bbox="808 354 1036 392">C0603(CC0201)</td> <td data-bbox="1036 354 1261 392"><math>\Delta T \leq 150</math></td> </tr> </tbody> </table> <p data-bbox="488 449 724 478">2. Cooling condition</p> <p data-bbox="532 487 1442 554">Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (<math>\Delta T</math>) must be less than 100°C.</p> <p data-bbox="488 600 716 630">5.5 Amount of solder</p> <p data-bbox="565 638 1442 741">Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.</p> <div data-bbox="540 785 656 852">Excessive solder</div> <div data-bbox="716 774 1101 873">  </div> <div data-bbox="1127 770 1373 869">Higher tensile force on the chip capacitor may cause cracking</div> <hr/> <div data-bbox="540 930 651 997">Adequate solder</div> <div data-bbox="716 909 1255 1008">  </div> <div data-bbox="540 1073 665 1140">Insufficient solder</div> <div data-bbox="716 1066 1101 1165">  </div> <div data-bbox="1127 1035 1382 1176">Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.</div> <p data-bbox="488 1220 828 1249">5.6 Solder repair by solder iron</p> <p data-bbox="488 1257 886 1287">1. Selection of the soldering iron tip</p> <p data-bbox="532 1295 1386 1465">Tip temperature of solder iron varies by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation, however, heat shock may cause a crack in the chip capacitor. Please confirm the tip temperature before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)</p> <p data-bbox="553 1497 1365 1526">Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)</p> <table border="1" data-bbox="581 1526 1362 1625"> <thead> <tr> <th data-bbox="581 1537 777 1575">Temp. (°C)</th> <th data-bbox="777 1537 972 1575">Duration (sec.)</th> <th data-bbox="972 1537 1167 1575">Wattage (W)</th> <th data-bbox="1167 1537 1362 1575">Shape (mm)</th> </tr> </thead> <tbody> <tr> <td data-bbox="581 1585 777 1623">300 max.</td> <td data-bbox="777 1585 972 1623">3 max.</td> <td data-bbox="972 1585 1167 1623">20 max.</td> <td data-bbox="1167 1585 1362 1623">Ø 3.0 max.</td> </tr> </tbody> </table>	Soldering	Type	Temp. (°C)	Reflow soldering	C0603(CC0201)	$\Delta T \leq 150$	Manual soldering	C0603(CC0201)	$\Delta T \leq 150$	Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	Ø 3.0 max.
Soldering	Type	Temp. (°C)																	
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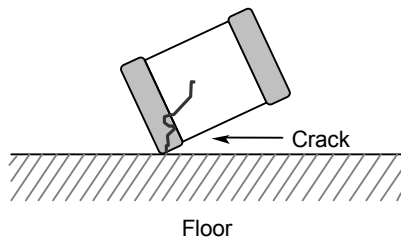
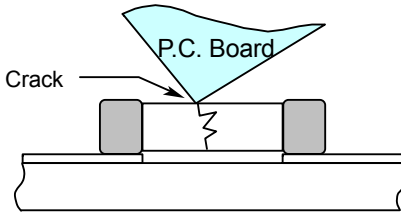
(10. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	<p>2. Direct contact of the soldering iron with ceramic dielectric of the chip capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5.7 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5.8 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially when the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 "Recommendations to prevent the tombstone phenomenon")</p>
6	Cleaning	<p>1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and deteriorate the insulation resistance.</p> <p>2. If cleaning condition is not suitable, it may deteriorate the chip capacitor's insulation resistance.</p> <p>2.1 Insufficient washing</p> <ol style="list-style-type: none"><li>1. Terminal electrodes may be corroded by Halogen in the flux.</li><li>2. Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance.</li><li>3. Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</li></ol> <p>2.2 Excessive washing</p> <p>When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended.</p> <p style="text-align: center;">Power: 20 W/ ℓmax. Frequency: 40 kHz max. Washing time: 5 minutes max.</p> <p>2.3 If the cleaning fluid is contaminated, the Halogen concentration increase and bring the same result as insufficient cleaning.</p>

(10. Caution, continued)

No.	Process	Condition						
7	Coating and molding of the P.C. Board	<ol style="list-style-type: none"> <li>When the P.C. board is coated, please verify the impact on the capacitor.</li> <li>Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor.</li> <li>Please verify the curing temperature.</li> </ol>						
8	Handling after chip mounted	<ol style="list-style-type: none"> <li>Please pay attention not to bend or distort the P.C. board after soldering otherwise the chip capacitor may crack.                     <div style="text-align: center; margin: 10px 0;">  </div> </li> <li>When functional check of the P.C. board is performed, higher pin pressure tends to be used for fear of loose contact. But if the pressure is excessive and bend the P.C. board, it may crack the chip capacitor or peel the terminations. Please adjust the pins accordingly to ensure the P.C. board is not flexed.                     <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th data-bbox="519 1039 649 1092">Item</th> <th data-bbox="649 1039 1039 1092">Not recommended</th> <th data-bbox="1039 1039 1412 1092">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="519 1092 649 1375">Board bending</td> <td data-bbox="649 1092 1039 1375">  </td> <td data-bbox="1039 1092 1412 1375">  </td> </tr> </tbody> </table> </li> </ol>	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								

(10. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitors	<p>1. The chip capacitor may crack if dropped, especially large case sizes. Please handle with care and do not use if dropped.</p>  <p>Floor</p> <p>Crack</p> <p>2. When stacking the P.C. board for storage or handling after soldering, the corner of the P.C. board may hit the chip capacitor of a neighboring board to cause a crack.</p>  <p>Crack</p> <p>P.C. Board</p>
10	Capacitance aging	Class 2 capacitors have an aging characteristic, which is a decrease in capacitance over time due to crystalline changes that occur in ferroelectric ceramics. Careful consideration should be done in case of a time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life and (failure rate) depend on the temperature and the voltage applied. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 "Calculation of the estimated lifetime and the estimated failure rate." The risk can be decreased by reducing the temperature and the voltage but they will not be guaranteed.
12	Others	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet:</p> <p>Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, ships, etc.) Medical equipment. Power-generation control equipment. Atomic energy-related equipment. Seabed equipment. Transportation control equipment.</p> <p>Public information-processing equipment. Military equipment. Electric heating apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose applications.</p> <p>When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup circuits, etc., to ensure higher safety.</p>

## 11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

\*Composition of Inspection No.

Example    M 0 A - 00 - 000  
                  (a) (b) (c)        (d)        (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

## 12. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.  
As for C0603 type, not available for bulk packaging.

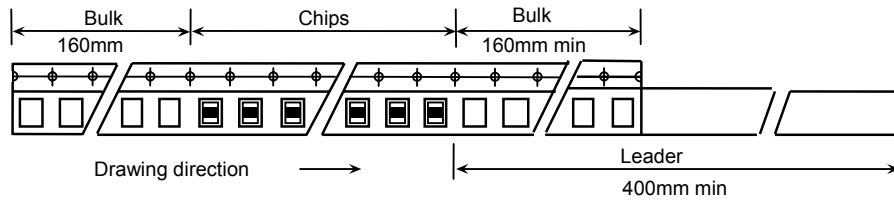
# 13. TAPE PACKAGING SPECIFICATION

## 1. CONSTRUCTION AND DIMENSION OF TAPING

### 1. Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 3.

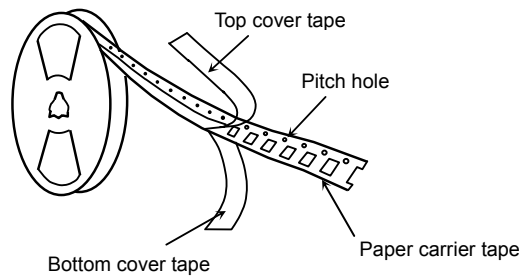
### 2. Bulk part and leader of taping



### 3. Dimensions of reel

Dimensions of  $\varnothing 178$  reel shall be according to Appendix 4.

### 4. Structure of taping

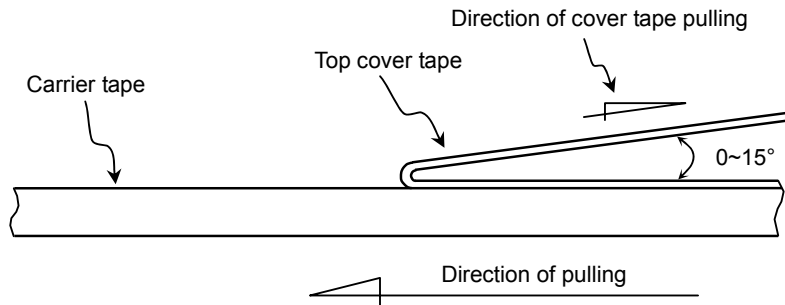


## 2. CHIP QUANTITY

Type	Thickness of chip	Taping Material	Chip quantity (pcs.)
			$\varnothing 178$ mm reel
C0603	0.30 mm	paper	15,000

### 3. PERFORMANCE SPECIFICATIONS

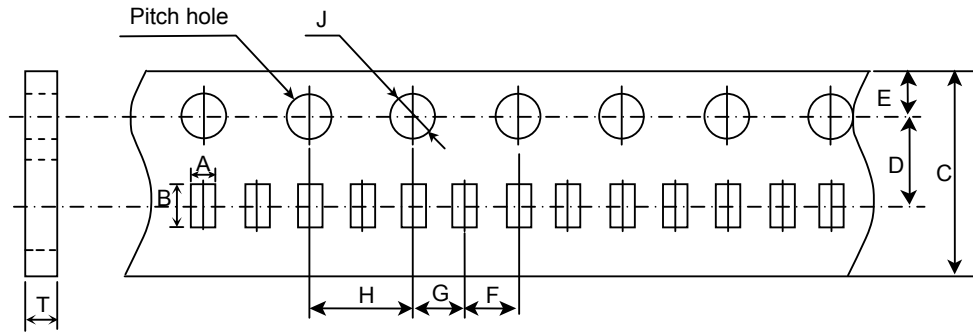
1. Peel back cover (top tape)  
0.05-0.7N. (See the following figure.)



2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.
3. The missing of components shall be less than 0.1%.
4. Components shall not stick to the cover tape.
5. The cover tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

### Appendix 3

#### Paper Tape



(Unit: mm)

Symbol	A	B	C	D	E	F
Type C0603 (CC0201)	( 0.38 )	( 0.68 )	$8.00 \pm 0.30$	$3.50 \pm 0.05$	$1.75 \pm 0.10$	$2.00 \pm 0.05$

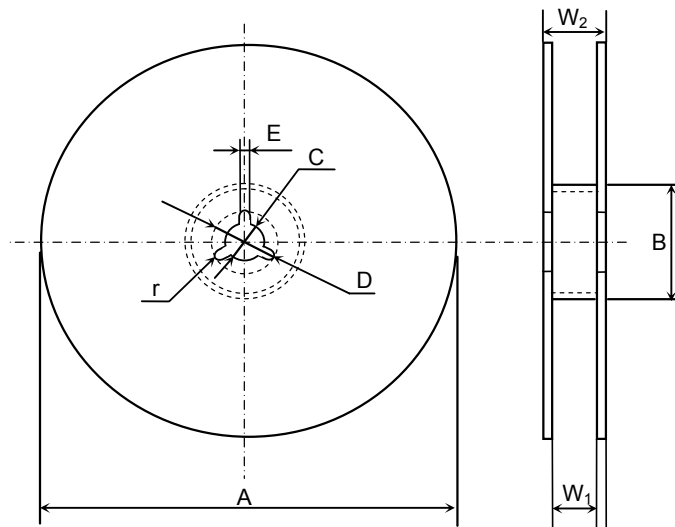
  

Symbol	G	H	J	T
Type C0603 (CC0201)	$2.00 \pm 0.05$	$4.00 \pm 0.10$	$\varnothing 1.5 \begin{smallmatrix} +0.10 \\ 0 \end{smallmatrix}$	0.40 min.

\* The values in the parentheses ( ) are for reference.

### Appendix 4

(Material: Polystyrene)



(Unit: mm)

Symbol	A	B	C	D	E	W <sub>1</sub>
Dimension	$\varnothing 178 \pm 2.0$	$\varnothing 60 \pm 2.0$	$\varnothing 13 \pm 0.5$	$\varnothing 21 \pm 0.8$	$2.0 \pm 0.5$	$9.0 \pm 0.3$

Symbol	W <sub>2</sub>	r
Dimension	$13.0 \pm 1.4$	1.0

END PAGE