SPECIFICATION

SPEC. No.

DATE :

Customer

CUSTOMER'S PRODUCT NAME	TDK PRODUCT NAME MULTILAYER CERAMIC CHIP CAPACITORS C4520, C4532 Type / 1.0kV to 3.0kV C0G, X7R Characteristics

Please sign and return this specification to local TDK representatives. If orders are placed without returned documentation, we must consider you found the specification acceptable.

THIS SPECIFICATION IS RECEIVED

DATE: YEAR MONTH DAY

TDK-EPC Corporation
1-13-1,Nihonbashi,Chuo-ku, Tokyo
103-0027,Japan

ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office

Sales Tel. ( )

PRODUCT CLASSIFICATION CODE	040320

1. SCOPE

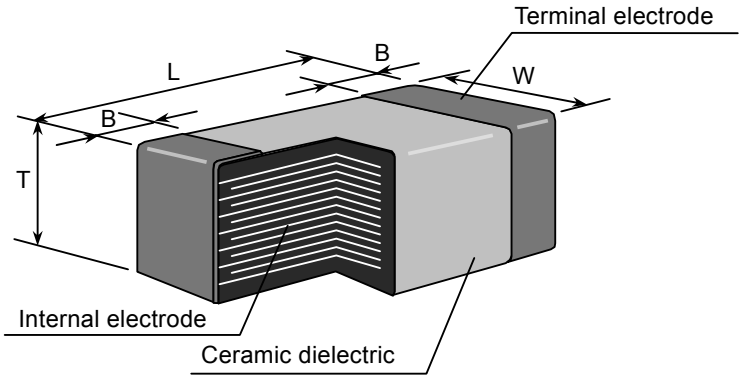
This specification is applicable to chip type multilayer ceramic capacitors with a priority over other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK-EPC HONG KONG LIMITED, TDK (Suzhou)Co., Ltd, TDK Malaysia) Sdn. Bhd, TDK Components U.S.A. Inc.

EXPLANATORY NOTE:
This specification warrants the quality of the TDK ceramic chip capacitors. The product should be evaluated and confirmed in your product before use. If the use of the product exceeds the bounds of this specification, we can not guarantee its quality and reliability.

2. CODE CONSTRUCTION

(Example)	C4532	X7R	3D	222	M	T
	(1)	(2)	(3)	(4)	(5)	(6)

1. Type



Please refer to product list for the dimensions of each product. See Section 9 for inside structure and material.

2. Temperature Characteristics (Details are shown in Section 8, No.7 and No.8)

3. Rated Voltage

Symbol	Rated Voltage
3 A	DC 1 kV
3 D	DC 2 kV
3 F	DC 3 kV

4. Rated Capacitance

Stated in three digits and in units of pico farads (pF). The first and second digits identify the first and second significant figures of the capacitance, the third digit identifies the multiplier. R is designated for a decimal point.

Example 222 → 2,200pF

5. Capacitance tolerance

Symbol	Tolerance	Capacitance
F	± 1 pF	10pF
K	± 10 %	Over 10pF
M	± 20 %	

6. Packaging

Symbol	Packaging
B	Bulk
T	Taping

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

1. Standard combination of rated capacitance and tolerances

Class	Temperature Characteristics	Capacitance tolerance		Rated capacitance
1	C0G	10pF	F (±1pF)	10
		Over 10pF	K (± 10 %)	E – 12 series
2	X7R	K (± 10 %)		E –3 series

2. Capacitance Step in E series

E series	Capacitance Step											
E- 3	1.0				2.2				4.7			
E- 12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X7R C0G	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

6. P.C. BOARD

When mounting on an aluminum substrate, large case sizes such as C4520 and C4532 types are more likely to be affected by heat stress from the substrate. Please inquire separate specification for the large case sizes when mounted on the substrate.

7. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

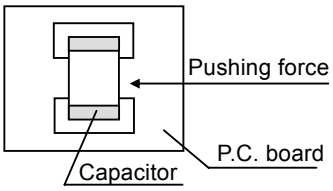
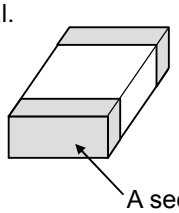
8. PERFORMANCE

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>1</td><td>External Appearance</td><td>No defects which may affect performance.</td><td>Inspect with magnifying glass (3×)</td></tr>
<tr><td>2</td><td>Insulation Resistance</td><td>10,000MΩ min.</td><td>Apply 500V DC for 60s.</td></tr>
<tr><td>3</td><td>Voltage Proof</td><td>Withstand test voltage without insulation breakdown or other damage.</td><td>1.2 times of rated voltage, above DC voltage shall be applied for 1 to 5s.

Charge / discharge current shall not exceed 50mA.</td></tr>
<tr><td>4</td><td>Capacitance</td><td>Within the specified tolerance.</td><td><table><tr><th>Class</th><th>Measuring frequency</th><th>Measuring voltage</th></tr><tr><td>Class 1</td><td>1MHz±10%</td><td>0.5 - 5 Vrms.</td></tr><tr><td>Class 2</td><td>1kHz±10%</td><td>1.0±0.2 Vrms.</td></tr></table></td></tr>
<tr><td>5</td><td>Q
(Class 1)</td><td><table><tr><th>Rated Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td><td>See No.4 in this table for measuring condition.</td></tr>
<tr><td>6</td><td>Dissipation Factor
(Class 2)</td><td><table><tr><th>T.C.</th><th>D.F.</th></tr><tr><td>X7R</td><td>0.03 max.</td></tr></table></td><td>See No.4 in this table for measuring condition.</td></tr>
</table>

(8. Performance, continued)

<table>
<tr><th>No.</th><th>Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td>7</td><td>Temperature Characteristics of Capacitance (Class 1)</td><td>
<table>
<tr><th>T.C.</th><th>Temperature Coefficient</th></tr>
<tr><td>C0G</td><td>0 ± 30 (ppm/°C)</td></tr>
</table>
Capacitance drift within ± 0.2% or ± 0.05pF, whichever larger.
</td><td>Temperature coefficient shall be calculated based on values at 25°C and 85°C temperature.

Measuring temperature below 20°C shall be -10°C and -25°C.</td></tr>
<tr><td>8</td><td>Temperature Characteristics of Capacitance (Class 2)</td><td>
<table>
<tr><th>Capacitance Change (%)</th></tr>
<tr><td>No voltage applied</td></tr>
<tr><td>X7R : ± 15</td></tr>
</table>
</td><td>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step.
ΔC be calculated ref. STEP3 reading
<table>
<tr><th>Step</th><th>Temperature(°C)</th></tr>
<tr><td>1</td><td>25 ± 2</td></tr>
<tr><td>2</td><td>-55 ± 3</td></tr>
<tr><td>3</td><td>25 ± 2</td></tr>
<tr><td>4</td><td>125 ± 2</td></tr>
</table>
</td></tr>
<tr><td>9</td><td>Robustness of Terminations</td><td>No sign of termination coming off, breakage of ceramic, or other abnormal signs.</td><td>Reflow solder the capacitors on P.C. board (shown in Appendix 1) and apply a pushing force of 5N with 10±1s.
 
</td></tr>
<tr><td>10</td><td>Solderability</td><td>New solder to cover over 75% of termination.
25% may have pin holes or rough spots but not concentrated in one spot.
Ceramic surface of “A sections” shall not be exposed due to melting or shifting of termination material.
 
</td><td>Completely soak both terminations in solder at 235±5°C for 2±0.5s.

Solder : H63A (JIS Z 3282)

Flux : Isopropyl alcohol (JIS K 8839)
Rosin(JIS K 5902) 25% solid solution.</td></tr>
</table>

(8. Performance, continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="4">11</td><td rowspan="4">Vibration</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="4">Reflow solder the capacitors on P.C. board (shown in Appendix 1) before testing.

Vibrate the capacitors with amplitude of
1.5mm P-P changing the frequencies from 10Hz to 55Hz and back to 10Hz in after 1min.
Repeat this for 2h each in 3 perpendicular directions.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class 1</td><td>C0G</td><td>± 2.5 %</td></tr><tr><td>Class 2</td><td>X7R</td><td>± 7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class 1)</td><td><table><tr><th>Rated Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class 2)</td><td>Meet the initial spec.</td></tr>
<tr><td rowspan="6">12</td><td rowspan="6">Temperature cycle</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="6">Reflow solder the capacitor on P.C. board (shown in Appendix 1) before testing.

Expose the capacitor in the conditions step1 through step 4 and repeat 5 times consecutively.

Leave the capacitor in ambient conditions for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.<table><tr><th>Step</th><th>Temperature(°C)</th><th>Time (min.)</th></tr><tr><td>1</td><td>-55 ± 3</td><td>30 ± 3</td></tr><tr><td>2</td><td>25 ± 2</td><td>2 - 5</td></tr><tr><td>3</td><td>125 ± 2</td><td>30 ± 2</td></tr><tr><td>4</td><td>25 ± 2</td><td>2 - 5</td></tr></table></td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class 1</td><td>C0G</td><td>±2.5 %</td></tr><tr><td>Class 2</td><td>X7R</td><td>±7.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class 1)</td><td><table><tr><th>Rated Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>1,000 min.</td></tr><tr><td>Under 30pF</td><td>400+20×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class 2)</td><td>Meet the initial spec.</td></tr>
<tr><td>Insulation Resistance</td><td>Meet the initial spec.</td></tr>
<tr><td>Voltage proof</td><td>No insulation breakdown or other damage.</td></tr>
</table>

(8. Performance, continued)

<table>
<tr><th>No.</th><th colspan="2">Item</th><th>Performance</th><th>Test or inspection method</th></tr>
<tr><td rowspan="5">13</td><td rowspan="5">Moisture Resistance (Steady State)</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on P.C. board (shown in Appendix 1) before testing.

Leave at temperature 40±2°C, 90 to 95%RH for 500 +24,0h.

Leave the capacitors in ambient conditions for 6 to 24h (Class 1) or 24±2h (Class 2) before measurement.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class 1</td><td>C0G</td><td>± 5 %</td></tr><tr><td>Class 2</td><td>X7R</td><td>±12.5 %</td></tr></table></td></tr>
<tr><td>Q
(Class 1)</td><td><table><tr><th>Rated Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>350 min.</td></tr><tr><td>10pF and over to under 30pF</td><td>275+5/2×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class 2)</td><td>Characteristics
X7R: 200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>1,000MΩ min.</td></tr>
<tr><td rowspan="5">14</td><td rowspan="5">Life</td><td>External appearance</td><td>No mechanical damage.</td><td rowspan="5">Reflow solder the capacitors on P.C. board (shown in Appendix 1) before testing.

Apply rated voltage at maximum operating temperature ±2°C for 1,000 +48, 0h.

Charge/discharge current shall not exceed 50mA.

Leave the capacitor in ambient conditions for 6 to 24h (Class1) or 24±2h (Class2) before measurement.

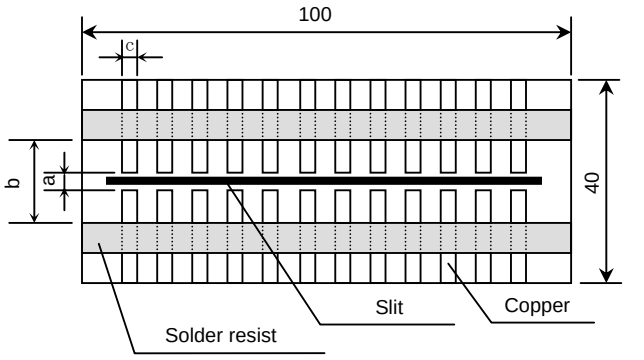
Voltage conditioning:
Voltage treat the capacitors under testing temperature and voltage for 1 hour.
Leave the capacitors in ambient condition for 24±2h before measurement.

Use this measurement for initial value.</td></tr>
<tr><td>Capacitance</td><td><table><tr><th colspan="2">Characteristics</th><th>Change from the value before test</th></tr><tr><td>Class 1</td><td>C0G</td><td>± 3 %</td></tr><tr><td>Class 2</td><td>X7R</td><td>±15 %</td></tr></table></td></tr>
<tr><td>Q
(Class 1)</td><td><table><tr><th>Rated Capacitance</th><th>Q</th></tr><tr><td>30pF and over</td><td>350 min.</td></tr><tr><td>10pF and over to under 30pF</td><td>275+5/2×C min.</td></tr></table>C : Rated capacitance (pF)</td></tr>
<tr><td>D.F.
(Class 2)</td><td>Characteristics
X7R: 200% of initial spec. max.</td></tr>
<tr><td>Insulation Resistance</td><td>1,000MΩ min.</td></tr>
</table>

*As for the initial measurement of capacitors (Class 2) on number 8, 11, 12 and 13, leave capacitors at 150 –10, 0°C for 1 hour and measure the value after leaving capacitor for 24±2h in ambient condition.

Appendix - 1

P.C. Board for reliability test



(Unit: mm)

Material: Glass Epoxy (As per JIS C6484 GE4)

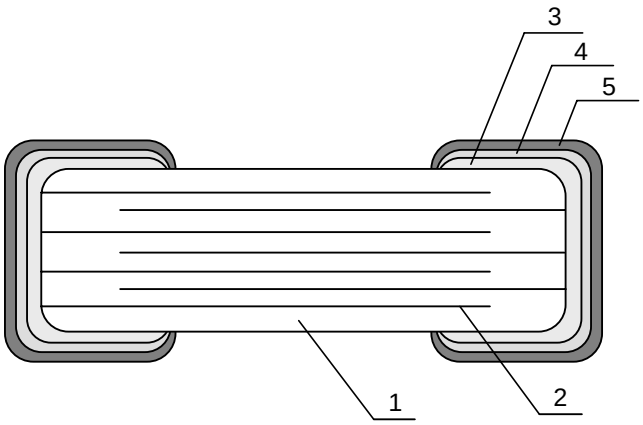
P.C. Board thickness: 1.6mm

Copper (thickness 0.035mm)

Solder resist

TDK (EIA style)	Dimensions (mm)		
	a	b	c
C4520	3.5	7.0	2.5
C4532	3.5	7.0	3.7

9. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL	
		Class 1	Class 2
1	Dielectric	$CaZrO_3$	$BaTiO_3$
2	Electrode	Nickel (Ni)	
3	Termination	Copper (Cu)	
4		Nickel (Ni)	
5		Tin (Sn)	

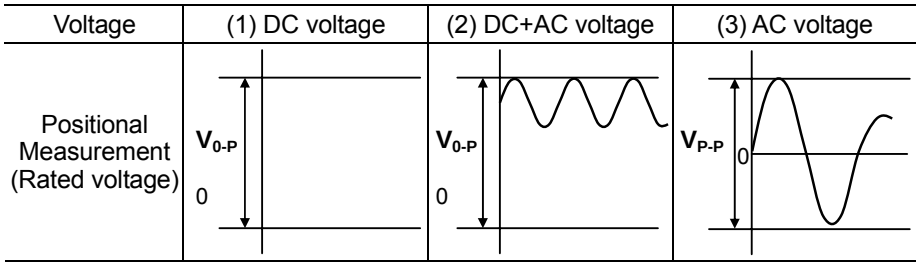
10. RECOMMENDATION

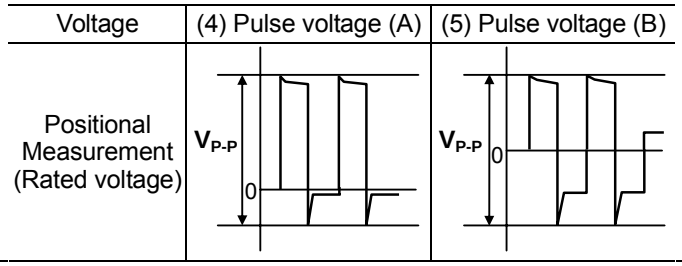
It is recommended to provide a slit (about 1mm wide) in the board under the components to improve washing flux. Please make sure to completely remove all cleaning solvents.

11. SOLDERING CONDITION

Reflow soldering only.

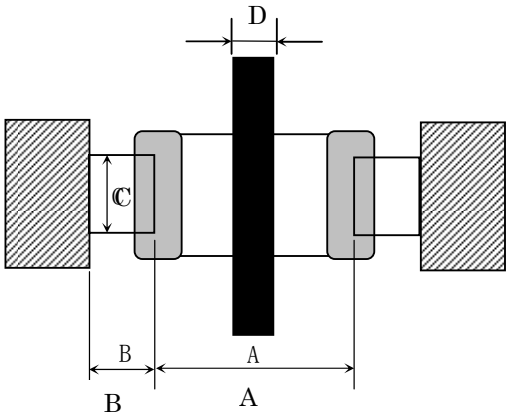
12. Caution

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>1</td><td>Operating Condition (Storage, Transportation)</td><td>1-1. Storage
1. The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt.
2. The capacitor must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur.
3. Avoid storing in sun light and falling of dew.
4. Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability
5. Capacitor should be tested for solderability when stored for long periods of time.
1.2 Handling in transportation
In case of the transportation, the performance of the capacitors may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 “Handling in Transportation”)</td></tr>
<tr><td>2</td><td>Circuit design</td><td>2.1 Operating temperature
Operating temperature should be followed strictly within this specification.
1. Do not use capacitors above the maximum allowable operating temperature.
2. Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product it’s mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C)
3. The electrical characteristics of the capacitor will vary depending on the temperature. The capacitor should be selected and designed after taking temperature into consideration.
2.2 Operating voltage
1. Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, $V_{0\text{-}P}$ must be below the rated voltage. Reference figures 1 and 2 below.
AC or pulse with overshooting, $V_{P\text{-}P}$ must be below the rated voltage. Reference figures 3, 4, and 5 below.
When the voltage is started/stopped to apply to the circuit an irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within its rated voltage during these Irregular voltage periods.
 


</td></tr>
</table>

(12. Caution, continued)

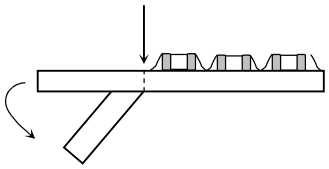
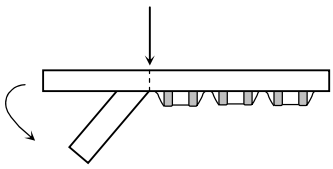
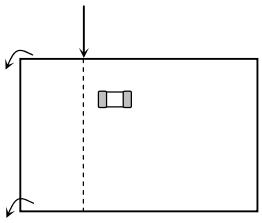
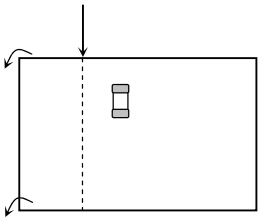
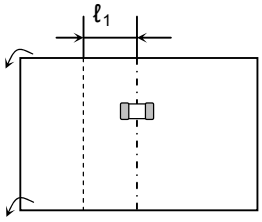
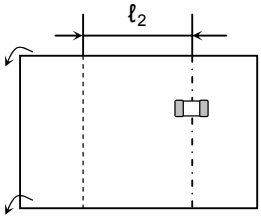
<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>2</td><td>Circuit design</td><td>2.2 Operating Voltage (continued)
2. Even below the rated voltage, if repetitive high AC frequency or pulsed is applied, the reliability of the capacitors may be reduced.
3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitor should be selected after considering the voltage affect.

2-3. Frequency
When Class 2 capacitors are used in AC and/or pulsed voltages, the capacitors may vibrate and generate audible sound (piezoelectric affect).</td></tr>
<tr><td>3</td><td>Designing
P.C. Board</td><td>The amount of solder at the terminations directly impacts the reliability of the capacitor.
1. The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder lands to have proper amount of solder on the terminations.
2. Avoid using common solder land for multiple terminations and provide individual solder land for each termination instead.
3. Size and recommended land dimensions provided below:
 

(mm)
<table>
<tr><th>Type / Symbol</th><th>C4520</th><th>C4532</th></tr>
<tr><td>A</td><td>3.1 - 3.7</td><td>3.1 - 3.7</td></tr>
<tr><td>B</td><td>1.2 - 1.4</td><td>1.2 - 1.4</td></tr>
<tr><td>C</td><td>1.5 - 2.0</td><td>2.4 - 3.2</td></tr>
<tr><td>D</td><td>1.0 - 1.3</td><td>1.0 - 1.3</td></tr>
</table></td></tr>
</table>

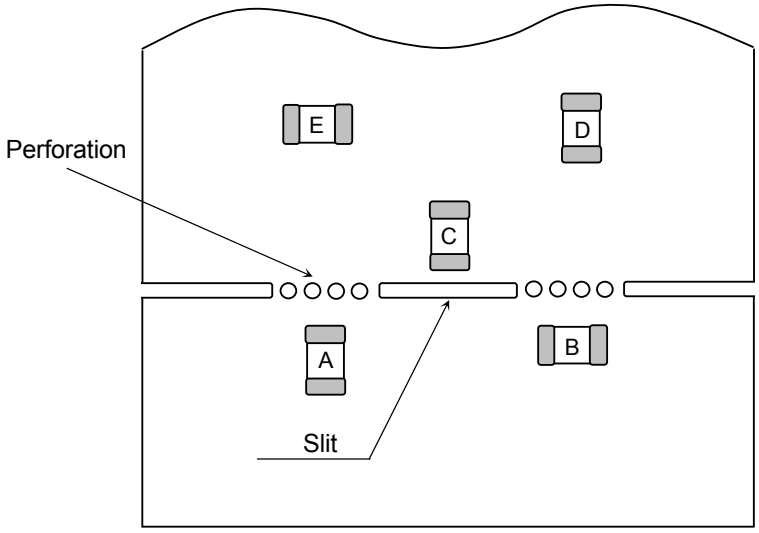
(12. Caution, continued)

No.	Process	Condition
3	Designing P.C. Board	4. Recommended chip capacitor layout is provided below:

	Disadvantage against bending stress	Advantage against bending stress
Mounting face	Perforation or slit  Break P.C. board with mounted side up.	Perforation or slit  Break P.C. board with mounted side down.
Chip arrangement (Direction)	Mount perpendicularly to perforation or slit Perforation or slit 	Mount in parallel with perforation or slit Perforation or slit 
Distance from slit	Closer to slit is higher stress  ($\ell_1 < \ell_2$)	Away from slit is less stress  ($\ell_1 < \ell_2$)

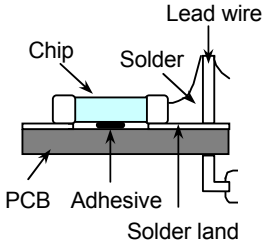
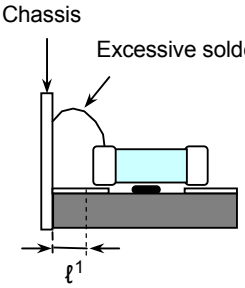
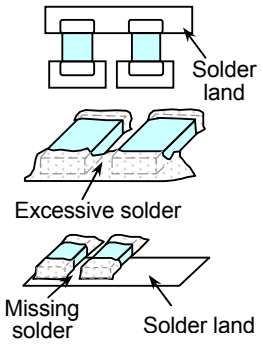
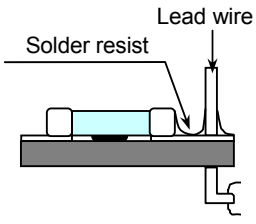
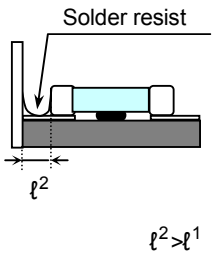
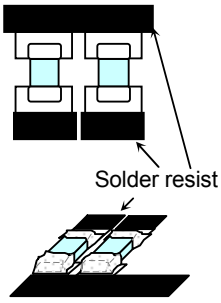
(12. Caution, continued)

No.	Process	Condition
3	Designing P.C. Board	5. Mechanical stress varies according to location of chip capacitor on the P.C. board.



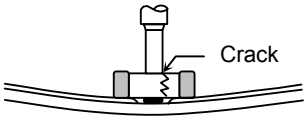
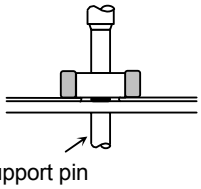
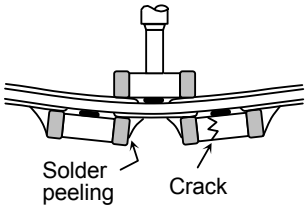
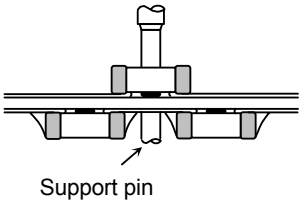
The relative stress applied to these capacitors during depaneling in the following order:
A > B = C > D > E

6. Layout recommendation

Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid			
Recommen-dation			

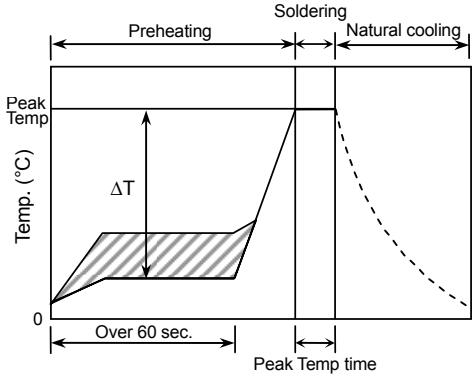
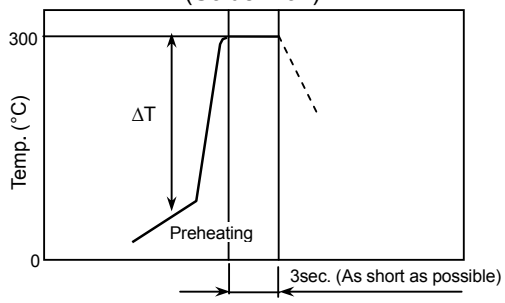
(12. Caution, continued)

No.	Process	Condition
4	Mounting	4.1 Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitor and result in cracking. Please take following precautions. 1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface but not contact it. 2. Adjust the mounting head pressure to be 1 to 3N of static weight. 3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board. See following examples.

	Not recommended	Recommended
Single sided mounting		
Double-sides mounting		

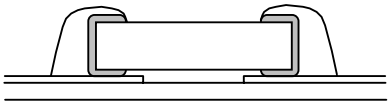
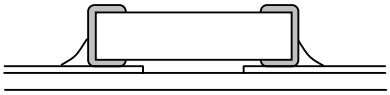
When the centering jaw is worn mechanical impact on the capacitor may occur and damage the product. Please control the closing dimension of the centering jaw and provide sufficient preventive maintenance and/or replacement if necessary.

(12. Caution, continued)

No.	Process	Condition
5	Soldering	5.1 Flux selection Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, the following is recommended. 1. Use a mildly activated rosin flux (less than 0.1wt% chlorine) . 2. Excessive flux must be avoided. Please provide proper amount of flux. 3. When water-soluble flux is used, sufficient washing is necessary. 5.2 Recommended soldering profile by various methods Reflow soldering  Manual soldering (Solder iron)  5.3 Recommended soldering peak temp and duration Temp./Duration / Solder Reflow soldering Peak temp(°C) / Duration(sec.) Sn-Pb Solder: 230 max. / 20 max. Lead Free Solder: 260 max. / 10 max. Recommended solder compositions Sn-37Pb (Sn-Pb solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)

(12. Caution, continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>5</td><td>Soldering
(continued)</td><td>
5.4. Avoiding thermal shock
1. Preheating condition
<table>
<tr><th>Soldering</th><th>Temp. (°C)</th></tr>
<tr><td>Reflow soldering</td><td>ΔT ≤ 130</td></tr>
<tr><td>Manual soldering</td><td>ΔT ≤ 130</td></tr>
</table>
2. Cooling condition
Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.

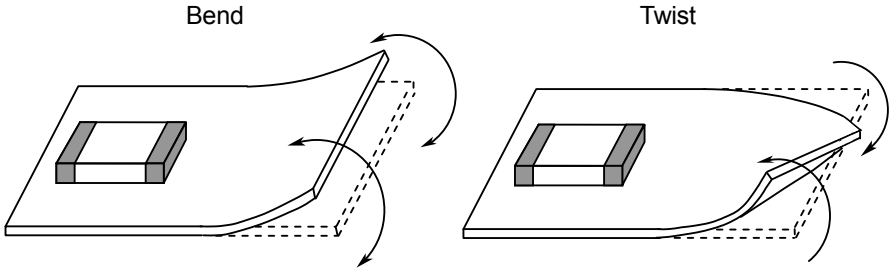
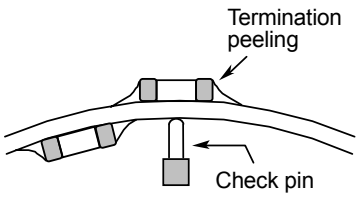
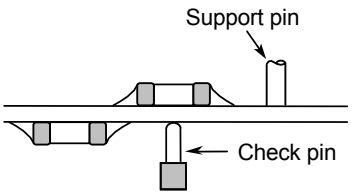
5.5 Amount of solder
Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. In sufficient solder may detach the capacitor from the P.C. board.
<table>
<tr><td>Excessive solder</td><td>  </td><td>Higher tensile force on the chip capacitor may cause cracking</td></tr>
<tr><td>Adequate</td><td>  </td><td></td></tr>
<tr><td>Insufficient solder</td><td>  </td><td>Small solder fillet may cause contact failure or not hold the chip capacitor come to the P.C. board.</td></tr>
</table>
5.6 Solder repair by solder iron
1. Selection of the soldering iron tip
Tip temperature of solder iron varies by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation; however, heat shock may cause a crack in the chip capacitor. Please confirm the tip temperature before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)

Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)
<table>
<tr><th>Temp. (°C)</th><th>Duration (sec.)</th><th>Wattage (W)</th><th>Shape (mm)</th></tr>
<tr><td>300 max.</td><td>3 max.</td><td>20 max.</td><td>Ø 3.0 max.</td></tr>
</table>
</td></tr>
</table>

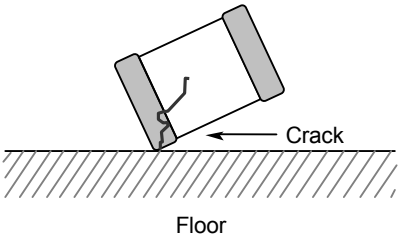
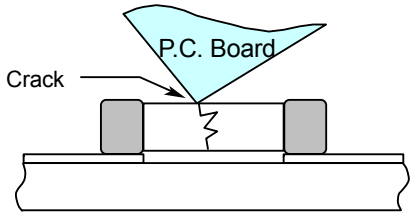
(12. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	2. Direct contact of the soldering iron with ceramic dielectric of the chip capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron. 5.7 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder. 5.8 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially when the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 “Recommendations to prevent the tombstone phenomenon”.)
6	Cleaning	1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and deteriorate the insulation resistance. 2. If cleaning condition is not suitable, it may deteriorate the chip capacitor’s insulation resistance. 2.1 Insufficient washing 1. Terminal electrodes may be corroded by Halogen in the flux. 2. Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance. 3. Water soluble flux has higher tendency to have above mentioned problems (1) and (2). 2.2 Excessive washing When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended. Power: 20 W/ℓ max. Frequency: 40 kHz max. Washing time: 5 minutes max. 2.3 If the cleaning fluid is contaminated, the Halogen concentration can increases, and brings the same result as insufficient cleaning.

(12. Caution, continued)

<table>
<tr><th>No.</th><th>Process</th><th>Condition</th></tr>
<tr><td>7</td><td>Coating and molding of the P.C. Board</td><td>1. When the P.C. board is coated, please verify the impact on the capacitor.
2. Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor.
3. Please verify the curing temperature.</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">Handling after chip mounted</td><td>1. Please pay attention not to bend or distort the P.C. board after soldering otherwise the chip capacitor may crack.
 
</td></tr>
<tr><td>2. When functional check of the P.C. board is performed, high pin pressure tends to be used for fear of loose contact. But if the pressure is excessive and bend the P.C. board, it may crack the chip capacitor or peel the terminations. Please adjust the pins accordingly to ensure the P.C. board is not flexed.
<table><tr><th>Item</th><th>Not recommended</th><th>Recommended</th></tr><tr><td>Board bending</td><td> 
</td><td> 
</td></tr></table></td></tr>
</table>

(12. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitors	1. The chip capacitor may crack if dropped, especially large case sizes. Please handle with care and do not use if dropped.  2. When stacking the P.C. board for storage or handling after soldering, the corner of the P.C. board may hit the chip capacitor of neighboring board to cause crack. 
10	Capacitance aging	Class 2 capacitors have an aging characteristic, which is a decrease in capacitance over time due to crystalline changes that occur in ferroelectric ceramics. Careful consideration should be done in case of a time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life and (failure rate) depend on the temperature And voltage applied. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 “Calculation of the estimated lifetime and the failure rate”. The risk can be decreased by reducing the temperature and the voltage but The failure rate can not be guaranteed.
12	Others	The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition. The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet: Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, ships, etc.) Medical equipment. Power-generation control equipment. Atomic energy-related equipment. Seabed equipment. Transportation control equipment. Public information-processing equipment. Military equipment. Electric heating apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose applications. When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup circuits, etc., to ensure higher safety.

13. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

1) Inspection No.
2) TDK P/N
3) Customer's P/N
4) Quantity

*Composition of Inspection No.

Example M 0 A – OO – OOO

(a) (b) (c) (d) (e)

a) Line code
b) Last digit of the year
c) Month and A for January and B for February and so on. (Skip I)
d) Inspection Date of the month.
e) Serial No. of the day

14. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

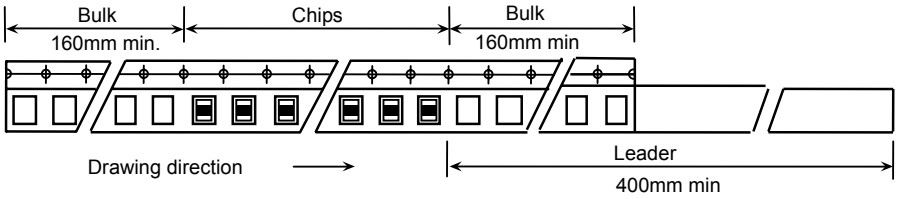
15. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1. 1 Dimensions of carrier tape

Dimensions of plastic tape shall be according to Appendix 2.

1. 2 Bulk part and leader of taping

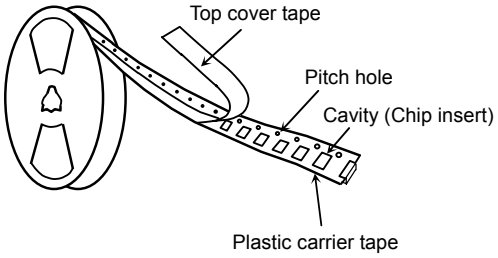


1. 3 Dimensions of reel

Dimensions of Ø178 reel shall be according to Appendix 3.

Dimensions of Ø330 reel shall be according to Appendix 4.

1. 4 Structure of taping



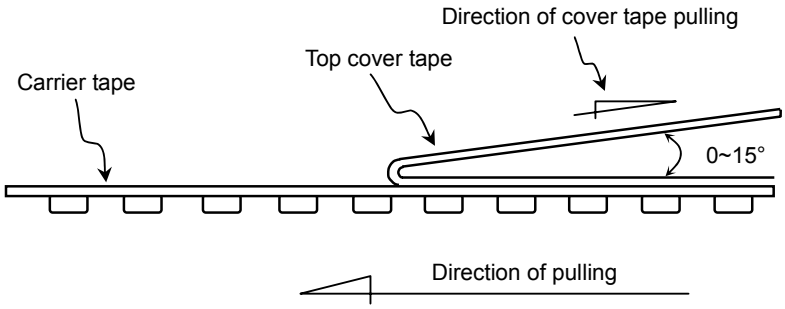
2. CHIP QUANTITY

Type	Thickness of chip	Taping Material	Chip quantity (pcs.)	Chip quantity (pcs.)
			φ178mm reel	φ330mm reel
C4520	0.85 mm	Plastic	1,000	5,000
	1.10 mm			
	1.30 mm			
	1.60 mm			3,000
	2.00 mm			
C4532	1.30 mm	Plastic	1,000	5,000
	1.60 mm			3,000
	2.00 mm			
	2.30 mm		500	
	2.50 mm			

3. PERFORMANCE SPECIFICATIONS

3. 1 Peel back cover (top tape)

0.05-0.7N. (See the following figure.)



3. 2 Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

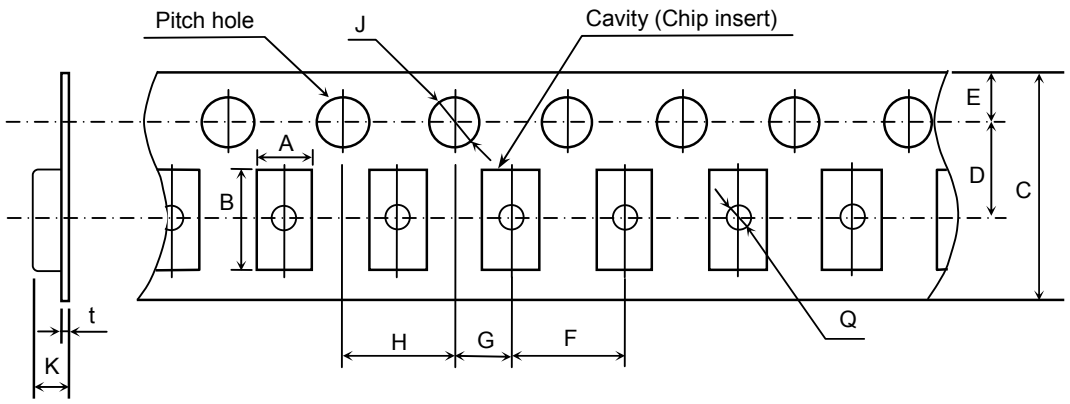
3. 3 The missing of components shall be less than 0.1%

3. 4 Components shall not stick to cover tape.

3. 5 The cover tapes shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 2

Plastic Tape



(Unit: mm)

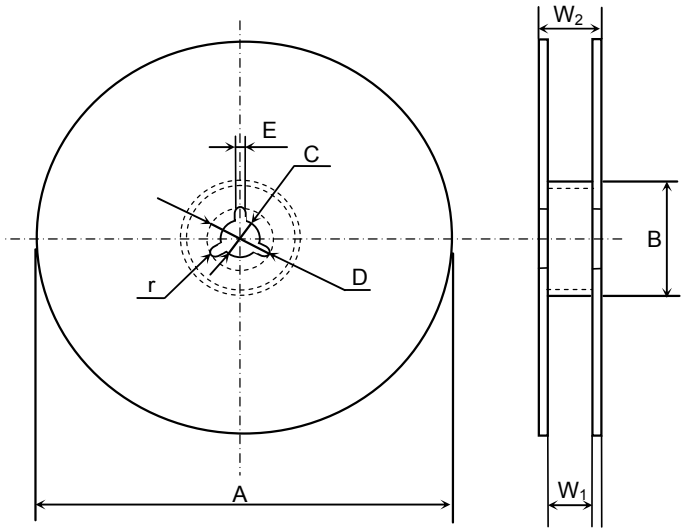
Symbol / Type	A	B	C	D	E	F
C4520	(2.50)	(5.10)	12.0 ± 0.30	5.50 ± 0.05	1.75 ± 0.10	8.00 ± 0.10
C4532	(3.60)	(4.90)				

Symbol / Type	G	H	J	K	t	Q
C4520	2.00 ± 0.05	4.00 ± 0.10	Ø 1.5 $^{+0.10}_{0}$	6.50 max.	0.60 max.	Ø 1.50 min.
C4532						

* The values in the parentheses ( ) are for reference.

Appendix 3

(Material: Polystyrene)



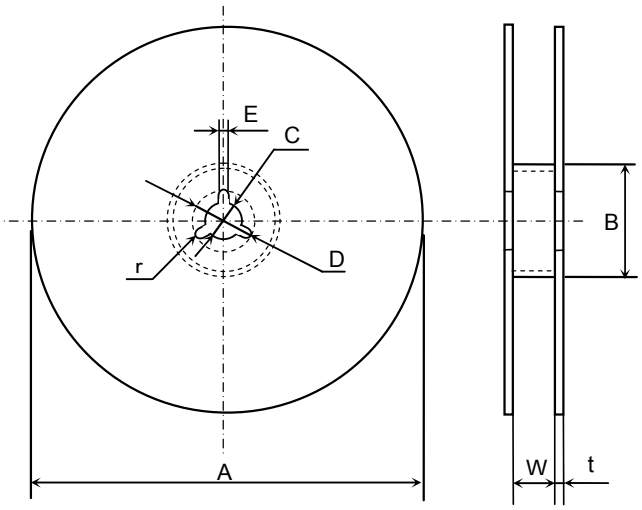
(Unit: mm)

Symbol	A	B	C	D	E	W_1
Dimension	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3

Symbol	W_2	r
Dimension	17.0 ± 1.4	1.0

Appendix 4

(Material: Polystyrene)



(Unit: mm)

Symbol	A	B	C	D	E	W
Dimension	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	14.0 ± 1.5

Symbol	t	r
Dimension	2.0 ± 0.5	1.0

END PAGE