



SPECIFICATION

SPEC. No. _____

DATE : _____

CUSTOMER'S PRODUCT NAME	TDK PRODUCT NAME MULTILAYER CERAMIC CHIP CAPACITORS CKG Type X5R, X7R, X7S, X7T Characteristics
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Please sign and return this specification to your local TDK representatives. If orders are placed without this returned documentation, we must consider you found the specification acceptable.

THIS SPECIFICATION IS RECEIVED

DATE: _____ YEAR _____ MONTH _____ DAY _____

TDK-EPC Corporation
1-13-1, Nihonbashi, Chuo-ku, Tokyo
103-0027, Japan

ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office _____

Sales Tel. () _____

PRODUCT CLASSIFICATION CODE	040320
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REV 0.3 /201012

1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co. ,Ltd, TDK-EPC HONG KONG LIMITED, TDK (Malaysia) Sdn. Bhd and TDK Components U.S.A. Inc.

EXPLANATORY NOTE:

This specification warrants the quality of the TDK ceramic chip capacitors. The product should be Evaluated and confirmed in on your product before use. If the use of the product exceeds the bounds of this specification, we can not guarantee its quality and reliability.

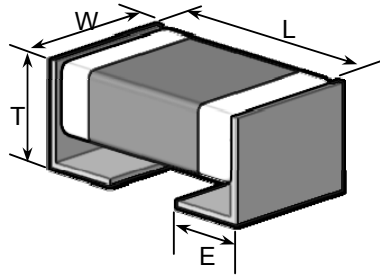
2. CODE CONSTRUCTION

(Example)	<u>CKG32K</u>	<u>X5R</u>	<u>1E</u>	<u>106</u>	<u>K</u>	<u>T</u>
	<u>CKG45N</u>	<u>X7R</u>	<u>1C</u>	<u>226</u>	<u>M</u>	<u>T</u>
	(1)	(2)	(3)	(4)	(5)	(6)

1. Type

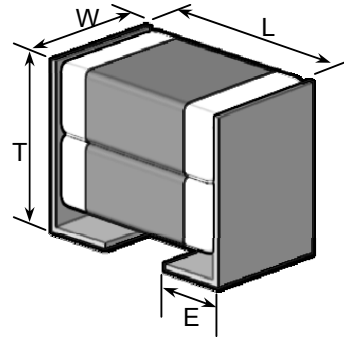
Single type

CKG**K: 1 chip capacitor.



Stacked type

CKG**N: 2 chip capacitors.



Please refer to product list for the dimension of each product. See Section 9 for inside structure and material.

2. Temperature Characteristics (Details are shown in Section 6, No.6)

3. Rated Voltage

Symbol	Rated Voltage
2 J	DC 630 V
2 W	DC 450 V
2 E	DC 250 V
2 A	DC 100 V
1 H	DC 50 V
1 E	DC 25 V
1 C	DC 16 V

4. Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and second digits identify the first and second significant figures of the capacitance; the third digit identifies the multiplier.

R is designated for a decimal point.

Example 106 → 10,000,000pF

226 → 22,000,000pF

5. Capacitance tolerance

Symbol	Tolerance
K ^{±1}	± 10 %
M	± 20 %(standard)

6. Packaging

Symbol	Packaging
T	Taping

3. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X5R	-55°C	85°C	25°C
X7R, X7S, X7T	-55°C	125°C	25°C

4. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH

6 months Max.

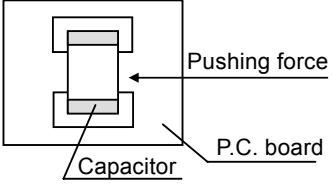
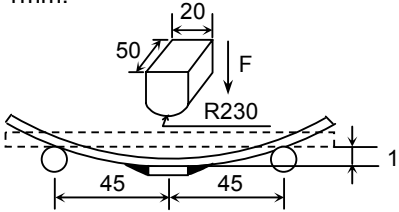
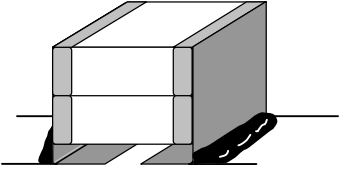
5. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

6. PERFORMANCE

No.	Item	Performance	Test or inspection method																				
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass (3X)																				
2	Insulation Resistance	500MΩ·μF min. (As for the capacitors of rated voltage 16V DC, 100MΩ·μF min.,) whichever smaller.	Apply rated voltage for 60s. As for the rated voltage 630V DC, apply 500V DC.																				
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	<table border="1"> <thead> <tr> <th>Rated voltage</th> <th>Apply voltage</th> </tr> </thead> <tbody> <tr> <td>100V and under</td> <td>2.5 × rated voltage</td> </tr> <tr> <td>Over 100V</td> <td>1.5 × rated voltage</td> </tr> </tbody> </table> <p>Above DC voltage shall be applied for 1 to 5s. Charge / discharge current shall not exceed 50mA.</p>	Rated voltage	Apply voltage	100V and under	2.5 × rated voltage	Over 100V	1.5 × rated voltage														
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100V and under	2.5 × rated voltage																						
Over 100V	1.5 × rated voltage																						
4	Capacitance	Within the specified tolerance.	<table border="1"> <thead> <tr> <th>Rated Capacitance</th> <th>Measuring frequency</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td>10uF and under</td> <td>1kHz±10%</td> <td>1.0±0.2Vrms.</td> </tr> <tr> <td>Over 10uF</td> <td>120Hz±20%</td> <td>0.5±0.2Vrms.</td> </tr> </tbody> </table>	Rated Capacitance	Measuring frequency	Measuring voltage	10uF and under	1kHz±10%	1.0±0.2Vrms.	Over 10uF	120Hz±20%	0.5±0.2Vrms.											
Rated Capacitance	Measuring frequency	Measuring voltage																					
10uF and under	1kHz±10%	1.0±0.2Vrms.																					
Over 10uF	120Hz±20%	0.5±0.2Vrms.																					
5	Dissipation Factor	<table border="1"> <thead> <tr> <th>T.C.</th> <th>D.F.</th> </tr> </thead> <tbody> <tr> <td>X5R</td> <td>0.045 max.</td> </tr> <tr> <td>X7R</td> <td>0.045 max.</td> </tr> <tr> <td>X7S</td> <td>0.075 max.</td> </tr> <tr> <td>X7T</td> <td>0.010 max.</td> </tr> </tbody> </table>	T.C.	D.F.	X5R	0.045 max.	X7R	0.045 max.	X7S	0.075 max.	X7T	0.010 max.	See No.4 in this table for measuring condition.										
T.C.	D.F.																						
X5R	0.045 max.																						
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6	Temperature Characteristics of Capacitance	<p>Capacitance Change (%)</p> <table border="1"> <thead> <tr> <th colspan="2">No voltage applied</th> </tr> </thead> <tbody> <tr> <td>X5R :</td> <td>± 15%</td> </tr> <tr> <td>X7R :</td> <td>±15%</td> </tr> <tr> <td>X7S :</td> <td>±22%</td> </tr> <tr> <td>X7T :</td> <td>+22%, -33%</td> </tr> </tbody> </table>	No voltage applied		X5R :	± 15%	X7R :	±15%	X7S :	±22%	X7T :	+22%, -33%	<p>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step. ΔC be calculated ref. STEP3 reading</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Reference temp. ± 2</td> </tr> <tr> <td>2</td> <td>Min. operating temp. ± 2</td> </tr> <tr> <td>3</td> <td>Reference temp. ± 2</td> </tr> <tr> <td>4</td> <td>Max. operating temp. ± 2</td> </tr> </tbody> </table>	Step	Temperature(°C)	1	Reference temp. ± 2	2	Min. operating temp. ± 2	3	Reference temp. ± 2	4	Max. operating temp. ± 2
No voltage applied																							
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Step	Temperature(°C)																						
1	Reference temp. ± 2																						
2	Min. operating temp. ± 2																						
3	Reference temp. ± 2																						
4	Max. operating temp. ± 2																						

(6. Performance, continued)

No.	Item	Performance	Test or inspection method
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	<p>Reflow solder the capacitors on P.C. board (shown in Appendix 1) and apply a pushing force of 5N with 10±1s.</p> 
8	Bending	No mechanical damage.	<p>Reflow solder the capacitors on P.C. board (shown in Appendix 2) and bend it for 1mm.</p>  <p style="text-align: right;">(Unit: mm)</p>
9	Solderability	<p>Both end faces and the contact areas shall be covered with a smooth and bright solder coating with no more than a small amount of scattered imperfections such as pinholes or un-wetted or de-wetted areas.</p> <p>These imperfections shall not be concentrated in one area.</p> 	<p>Reflow solder the capacitors on P.C. board (shown in Appendix 1).</p> <p>Solder : H63A (JIS Z 3282)</p> <p>Flux : Isopropyl alcohol (JIS K 8839) Rosin(JIS K 5902) 25% solid solution.</p>

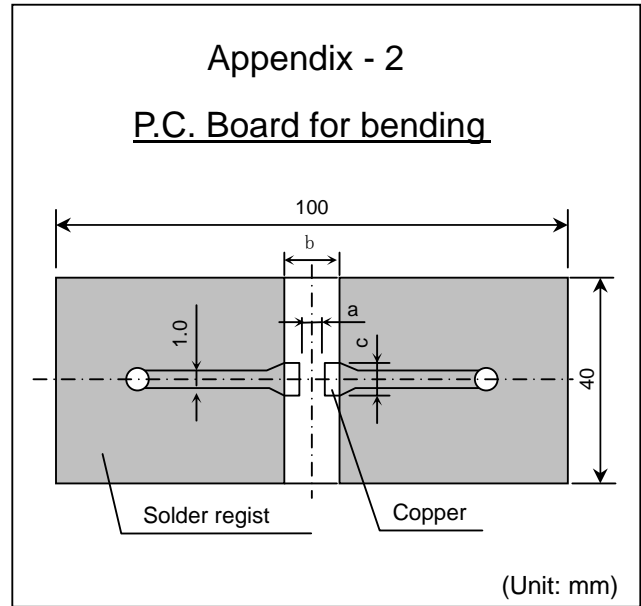
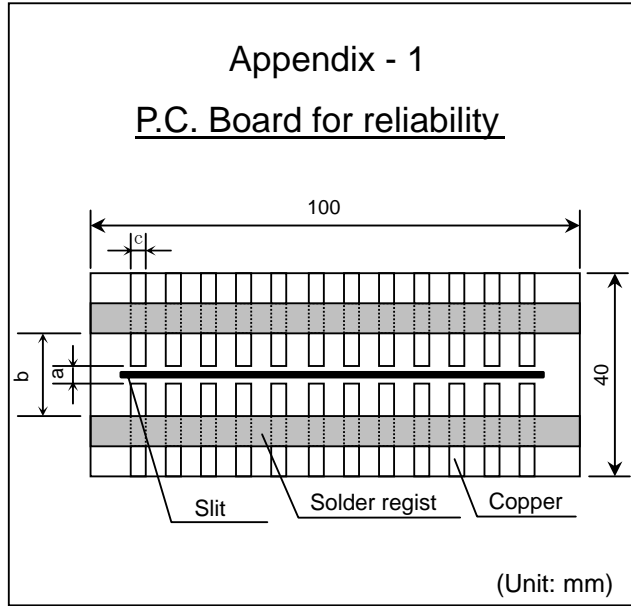
(6. Performance, continued)

No.	Item		Performance	Test or inspection method																
10	Temperature Cycle	External appearance	No mechanical damage.	Reflow solder the capacitors on P.C. board (shown in Appendix 1) before testing. Expose the capacitors in the condition step1 through step 4 and repeat 100 times consecutively. Leave the capacitors in ambient condition for 24±2h before measurement.																
		Capacitance	Characteristics		Change from the value before test															
			X5R X7R X7S X7T		± 7.5 %															
		D.F.	Meet the initial spec.		<table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> <th>Time (min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating temp. ± 3</td> <td>30 ± 3</td> </tr> <tr> <td>2</td> <td>Reference temp. ± 2</td> <td>2 - 5</td> </tr> <tr> <td>3</td> <td>Max. operating temp. ± 2</td> <td>30 ± 2</td> </tr> <tr> <td>4</td> <td>Reference temp. ± 2</td> <td>2 - 5</td> </tr> </tbody> </table>	Step	Temperature(°C)	Time (min.)	1	Min. operating temp. ± 3	30 ± 3	2	Reference temp. ± 2	2 - 5	3	Max. operating temp. ± 2	30 ± 2	4	Reference temp. ± 2	2 - 5
		Step	Temperature(°C)		Time (min.)															
1	Min. operating temp. ± 3	30 ± 3																		
2	Reference temp. ± 2	2 - 5																		
3	Max. operating temp. ± 2	30 ± 2																		
4	Reference temp. ± 2	2 - 5																		
Insulation Resistance	Meet the initial spec.																			
Voltage proof	No insulation breakdown or other damage.																			
11	Moisture Resistance	External appearance	No mechanical damage.	Reflow solder the capacitors on a P.C. board (shown in Appendix 1) before testing. Apply the rated voltage at temperature 40±2°C and 90 to 95%RH for 500 +24,0h. Charge/discharge current shall not exceed 50mA. Leave the capacitor in ambient conditions for 24±2h before measurement. Voltage conditioning: Voltage treats the capacitor under testing temperature and voltage for 1 hour. Leave the capacitor in ambient conditions for 24±2h before measurement. Use this measurement for initial value.																
		Capacitance	Characteristics		Change from the value before test															
			X5R X7R X7S X7T		± 12.5 %															
D.F.	Characteristics X5R/X7R/X7S/X7T : 200% of initial spec. max.																			
Insulation Resistance	25MΩ·μF min. (As for the capacitors of rated voltage 16V DC, 5MΩ·μF min.,).																			

(6. Performance, continued)

No.	Item	Performance	Test or inspection method				
12	Life	External appearance	No mechanical damage.				
	Life	Capacitance	<table border="1"> <thead> <tr> <th data-bbox="571 304 760 373">Characteristics</th> <th data-bbox="760 304 964 373">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="571 373 760 497">X5R X7R X7S X7T</td> <td data-bbox="760 373 964 497">± 15 %</td> </tr> </tbody> </table>	Characteristics	Change from the value before test	X5R X7R X7S X7T	± 15 %
		Characteristics	Change from the value before test				
	X5R X7R X7S X7T	± 15 %					
D.F.	Characteristics X5R/X7R/X7S/X7T : 200% of initial spec. max.						
Insulation Resistance	50MΩ·μF min. (As for the capacitors of rated voltage 16V DC, 10MΩ·μF min.,)						
			Reflow solder the capacitors on a P.C.Board shown in Appendix 1 before testing. Below the voltage shall be applied at Maximum operating temperature ±2°C for 1,000 +48, 0h. Applied voltage is 1xRV. Some items may be tested at higher voltage (1.2x, 1.5x or 2xRV). Charge/discharge current shall not exceed 50mA. Leave the capacitors in ambient condition for 24±2h before measurement. Voltage conditioning: Voltage treat the capacitors under testing temperature and voltage for 1 hour. Leave the capacitors in ambient condition for 24±2h before measurement. Use this measurement for initial value.				

*As for the initial measurement of capacitors on number 6 and 10, leave capacitors at 150 –10, 0°C for 1 hour and measure the value after leaving capacitors for 24±2h in ambient condition.



(Unit : mm)

Type	Dimensions		
	a	b	c
TDK(EIA style)			
CKG32K	2.2	5.0	2.9
CKG45K	3.5	6.1	2.9
CKG57K	4.1	7.6	4.7
CKG45N	3.5	6.1	2.9
CKG57N	4.1	7.6	4.7

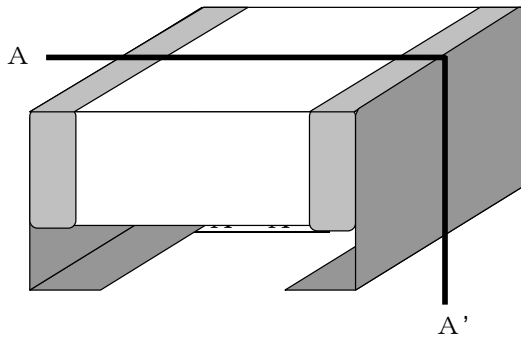
1. Material : Glass Epoxy(As per JIS C6484 GE4)

2. Thickness : 1.6mm

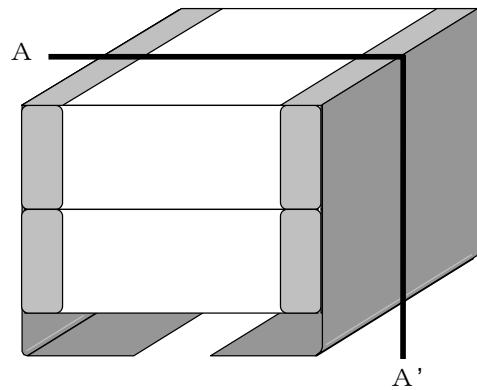
Copper(Thickness:0.035mm)
 Solder resist

7. INSIDE STRUCTURE AND MATERIAL

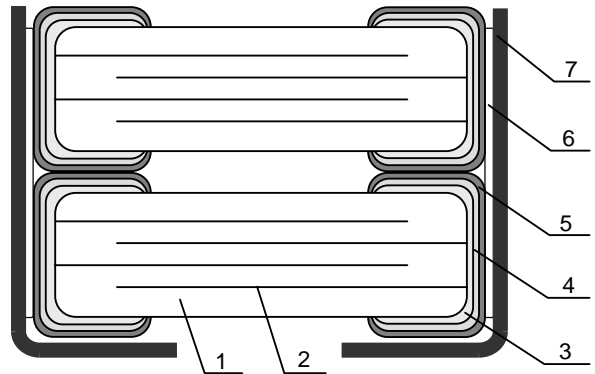
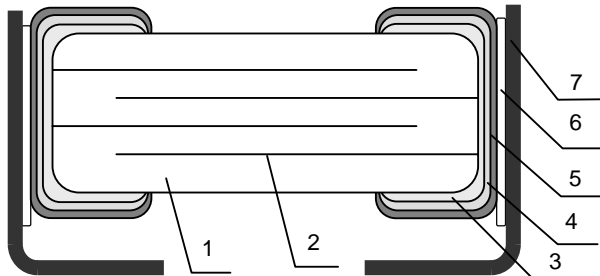
CKGK: Single**
(1 chip capacitor)



CKGN: Double**
(2 chip capacitors)



A - A'



No.	NAME	MATERIAL
1	Dielectric	BaTiO ₃
2	Electrode	Nickel (Ni)
3	Termination	Copper (Cu)
4		Nickel (Ni)
5		Tin (Sn)
6	Metal cap joint	High temp solder
7	Metal cap	42 Alloy

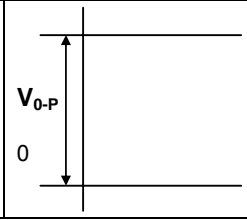
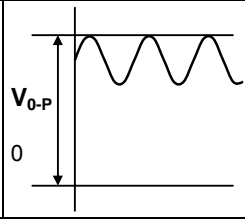
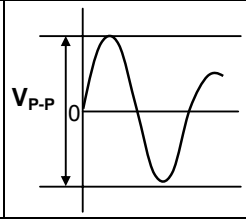
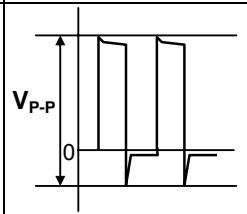
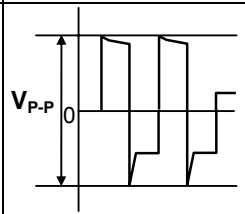
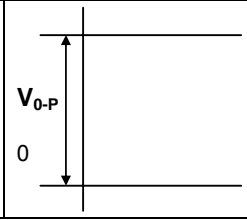
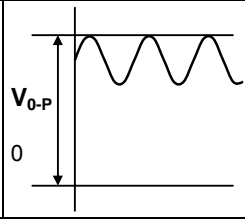
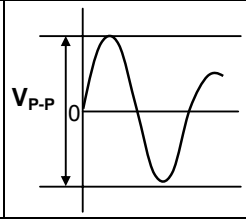
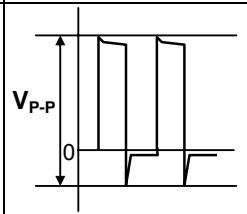
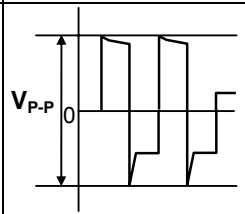
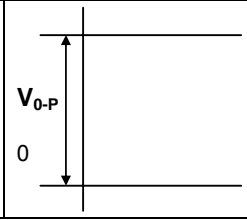
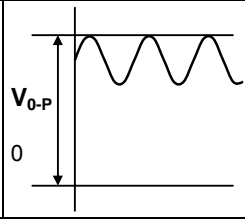
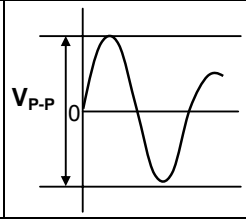
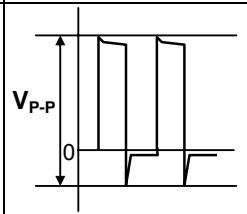
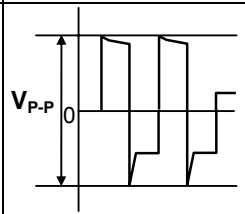
8. RECOMMENDATION

It is recommended to provide a slit (about 1mm wide) in the board under the components to improve washing flux. Please make sure to completely remove all cleaning solvents.

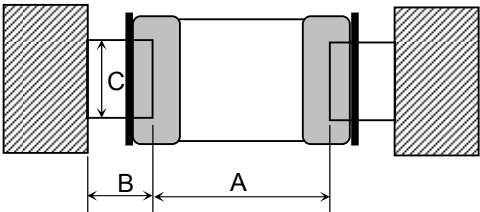
9. SOLDERING CONDITION

Reflow soldering only. "Metal cap joint" is high temperature solder, but it may be melted under high temperature (more than 250°C). Please keep a soldering temperature of 250°C or less and refer to "CAUTION" on No.5 in detail.

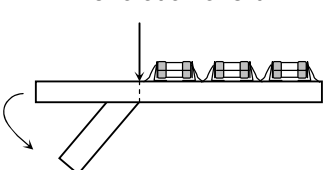
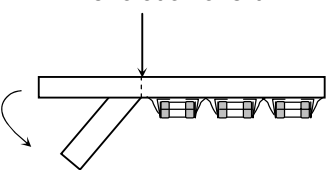
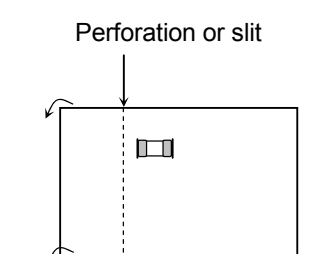
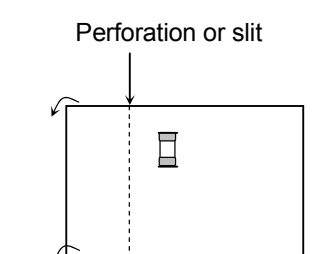
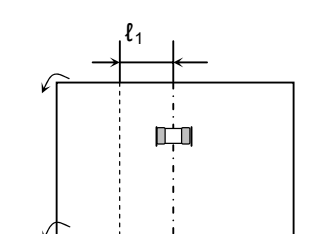
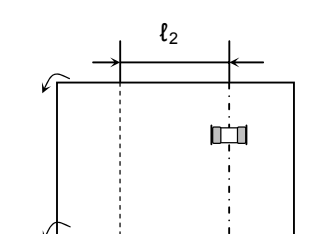
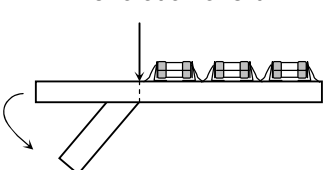
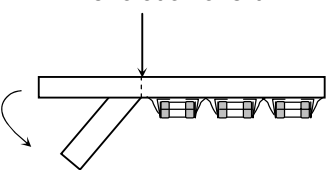
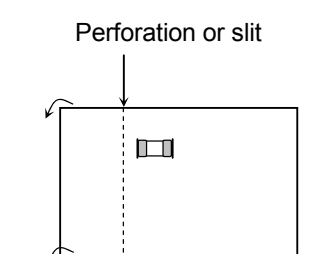
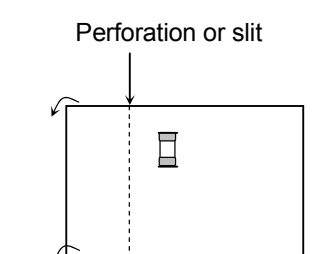
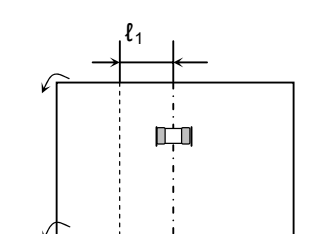
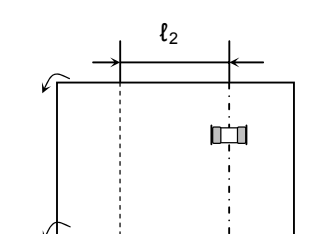
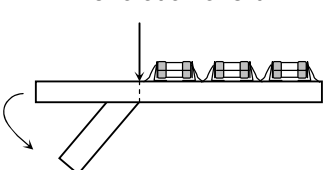
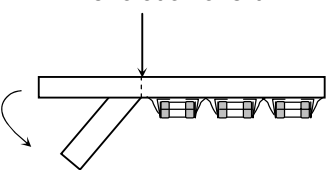
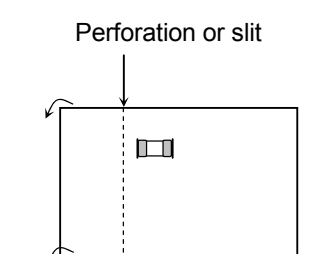
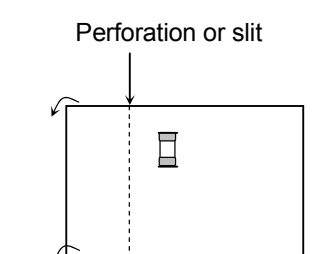
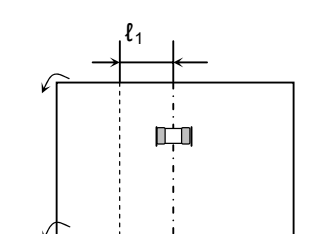
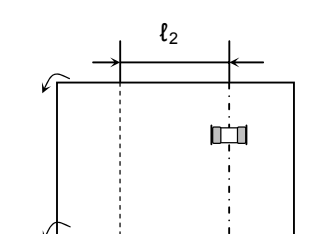
10. Caution

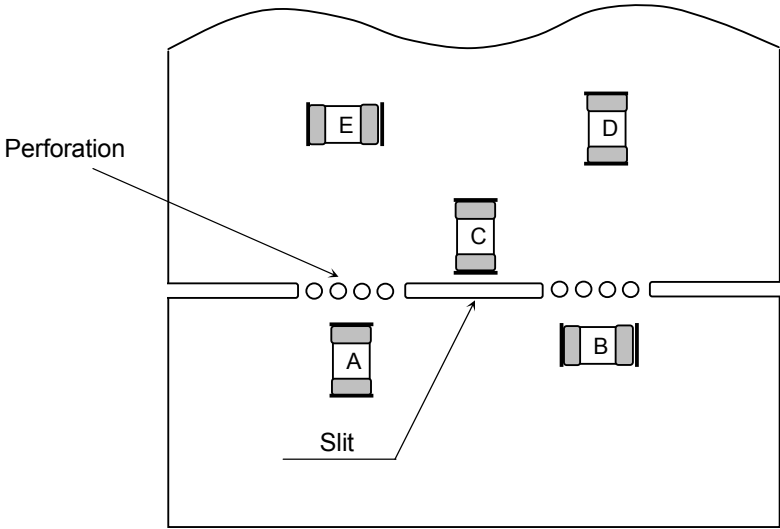
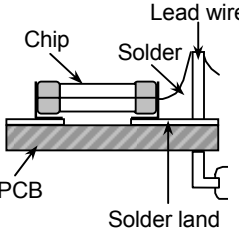
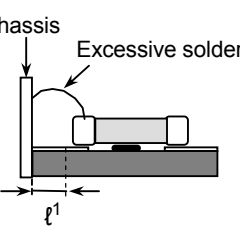
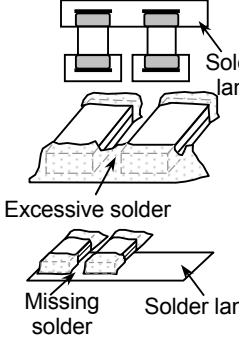
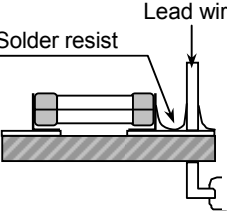
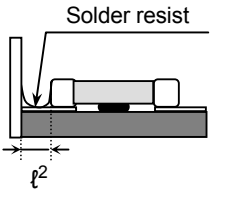
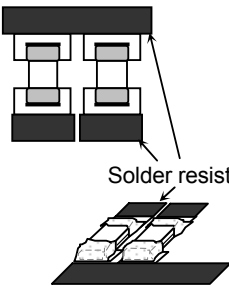
No.	Process	Condition																
1	Operating Condition (Storage, Transportation)	<p>1.1 Storage</p> <ol style="list-style-type: none"> The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt. The capacitor must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur. Avoid storing in sun light and falling of dew. Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability. Capacitor should be tested for solderability when stored for long period of time. <p>1.2 Handling in transportation</p> <p>In case of the transportation, the performance of the capacitor may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 "Handling in Transportation")</p>																
2	Circuit design	<p>2.1 Operating temperature</p> <p>Operating temperature should be followed strictly within this specification,</p> <ol style="list-style-type: none"> Do not use capacitors above the maximum allowable operating temperature. Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product it's mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) The electrical characteristics of the capacitor will vary depending on the temperature. The capacitor should be selected and designed after taking temperature into consideration. <p>2.2 Operating voltage</p> <ol style="list-style-type: none"> Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. Reference figures 1 and 2 below. AC or pulse with overshooting, V_{P-P} must be below the rated voltage. References figures 3, 4 and 5 below. When the voltage is started/stopped to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within its rated voltage during these Irregular voltage periods. <table border="1" data-bbox="505 1360 1414 1894"> <thead> <tr> <th data-bbox="505 1360 683 1402">Voltage</th> <th data-bbox="683 1360 927 1402">(1) DC voltage</th> <th data-bbox="927 1360 1170 1402">(2) DC+AC voltage</th> <th data-bbox="1170 1360 1414 1402">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="505 1402 683 1619">Positional Measurement (Rated voltage)</td> <td data-bbox="683 1402 927 1619">  </td> <td data-bbox="927 1402 1170 1619">  </td> <td data-bbox="1170 1402 1414 1619">  </td> </tr> <tr> <th data-bbox="505 1640 683 1682">Voltage</th> <th data-bbox="683 1640 927 1682">(4) Pulse voltage (A)</th> <th data-bbox="927 1640 1170 1682">(5) Pulse voltage (B)</th> <th></th> </tr> <tr> <td data-bbox="505 1682 683 1894">Positional Measurement (Rated voltage)</td> <td data-bbox="683 1682 927 1894">  </td> <td data-bbox="927 1682 1170 1894">  </td> <td></td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)		Positional Measurement (Rated voltage)			
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(10. Caution, continued)

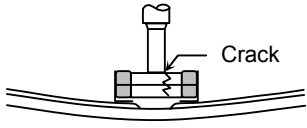
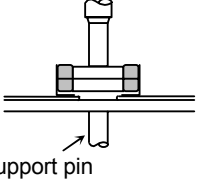
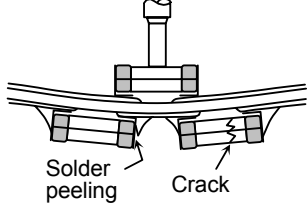
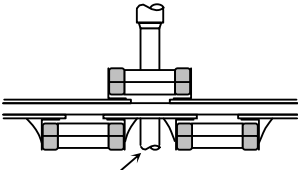
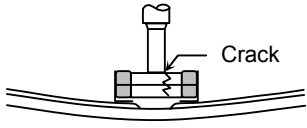
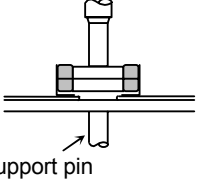
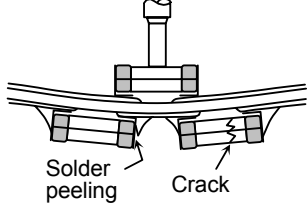
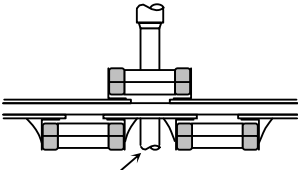
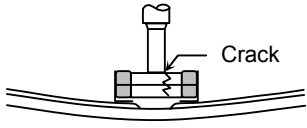
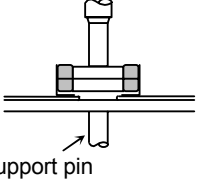
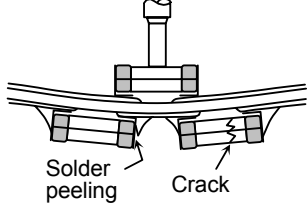
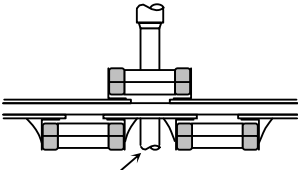
No.	Process	Condition																
2	Circuit design	<p>2.2 Operating voltage (continued)</p> <p>2. Even below the rated voltage, if repetitive high AC frequency or pulsed voltage is applied, the reliability of the capacitors may be reduced.</p> <p>3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitor should be selected after considering the voltage affect.</p> <p>2.3 Frequency</p> <p>When Class 2 the capacitors are used in AC and/or pulsed voltages, the capacitors may self vibrate and generate audible sound (piezoelectric affect).</p>																
3	Designing P.C. Board	<p>The amount of solder at the terminations has a direct effect on the reliability of the Capacitor.</p> <p>1. The greater the amount of solder, the higher the stress on the chip capacitor, And the more likely that it will break. When designing a P.C.board, determine the shape and size of the solder lands to have proper amount of solder on the Terminations.</p> <p>2. Avoid using common solder land for multiple terminations and provide individual Solder land for each termination instead.</p> <p>3. Size and recommended land dimensions provided below:</p> <div style="text-align: center;">  </div> <p style="text-align: right;">(mm)</p> <table border="1" data-bbox="532 1083 1276 1289"> <thead> <tr> <th>Type Symbol</th> <th>CKG32K</th> <th>CKG45K CKG45N</th> <th>CKG57K CKG57N</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>2.0 – 2.2</td> <td>3.3 – 3.7</td> <td>3.9 – 4.3</td> </tr> <tr> <td>B</td> <td>1.1 - 1.3</td> <td>1.2 - 1.5</td> <td>1.5 – 2.0</td> </tr> <tr> <td>C</td> <td>2.3 – 2.5</td> <td>2.7 – 3.2</td> <td>4.5 – 5.0</td> </tr> </tbody> </table>	Type Symbol	CKG32K	CKG45K CKG45N	CKG57K CKG57N	A	2.0 – 2.2	3.3 – 3.7	3.9 – 4.3	B	1.1 - 1.3	1.2 - 1.5	1.5 – 2.0	C	2.3 – 2.5	2.7 – 3.2	4.5 – 5.0
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(12. Caution, continued)

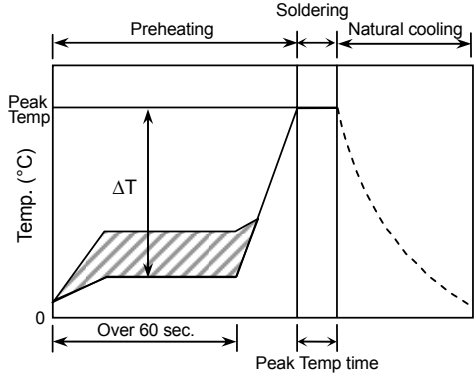
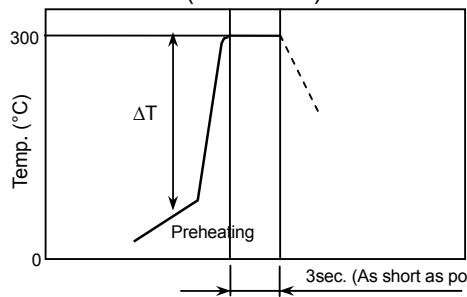
No.	Process	Condition												
3	Designing P.C. board (continued)	<p>4. Recommended chip capacitor layout is provided below:</p> <table border="1"> <thead> <tr> <th data-bbox="506 235 683 310"></th> <th data-bbox="683 235 1040 310">Disadvantage against bending stress</th> <th data-bbox="1040 235 1398 310">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="506 310 683 701">Mounting face</td> <td data-bbox="683 310 1040 701"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p> </td> <td data-bbox="1040 310 1398 701"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="506 701 683 1121">Chip arrangement (Direction)</td> <td data-bbox="683 701 1040 1121"> <p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p>  </td> <td data-bbox="1040 701 1398 1121"> <p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="506 1121 683 1570">Distance from slit</td> <td data-bbox="683 1121 1040 1570"> <p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p> </td> <td data-bbox="1040 1121 1398 1570"> <p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p>	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p>	Chip arrangement (Direction)	<p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p> 	<p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p> 	Distance from slit	<p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p>	<p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p>
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No.	Process	Condition	
3	Designing P.C. Board (continued)	<p>5. Mechanical stress varies according to location of chip capacitor on the P.C.board.</p>  <p>The relative stress applied to these capacitors during depaneling is in the following order.</p> $A > B = C > D > E$	
6. Layout recommendation			
Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Need to avoid			
Recommendation		 <p>$l^2 > l^1$</p>	

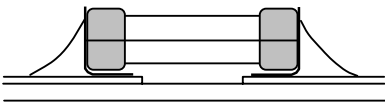
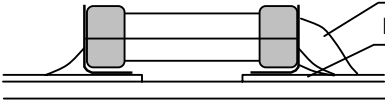
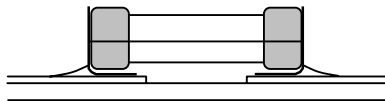
(12. Caution, continued)

No.	Process	Condition									
4	Mounting	<p data-bbox="483 170 1425 264">4.1 Stress from mounting head If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitors and result in cracking. Please take following precautions.</p> <ol data-bbox="483 296 1425 512" style="list-style-type: none"><li data-bbox="483 296 1425 359">1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface but not contact it..<li data-bbox="483 390 1425 422">2. Adjust the mounting head pressure to be 1 to 3N of static weight.<li data-bbox="483 453 1425 512">3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C.board. <p data-bbox="516 527 786 552">See following examples.</p> <table border="1" data-bbox="516 562 1403 1094"><thead><tr><th data-bbox="516 562 686 611"></th><th data-bbox="686 562 1057 611">Not recommended</th><th data-bbox="1057 562 1403 611">Recommended</th></tr></thead><tbody><tr><td data-bbox="516 611 686 842">Single sided mounting</td><td data-bbox="686 611 1057 842"><p data-bbox="943 709 1003 737">Crack</p></td><td data-bbox="1057 611 1403 842"><p data-bbox="1110 806 1224 833">Support pin</p></td></tr><tr><td data-bbox="516 842 686 1094">Double-sides mounting</td><td data-bbox="686 842 1057 1094"><p data-bbox="769 1052 846 1079">Solder peeling</p><p data-bbox="894 1052 954 1079">Crack</p></td><td data-bbox="1057 842 1403 1094"><p data-bbox="1081 1052 1195 1079">Support pin</p></td></tr></tbody></table> <p data-bbox="500 1129 1425 1224">When the centering jaw is worn out, it may give mechanical impact on the capacitors to cause crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.</p>		Not recommended	Recommended	Single sided mounting	 <p data-bbox="943 709 1003 737">Crack</p>	 <p data-bbox="1110 806 1224 833">Support pin</p>	Double-sides mounting	 <p data-bbox="769 1052 846 1079">Solder peeling</p> <p data-bbox="894 1052 954 1079">Crack</p>	 <p data-bbox="1081 1052 1195 1079">Support pin</p>
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(12. Caution, continued)

No.	Process	Condition														
5	Soldering	<p>5.1 Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, the following is recommended.</p> <ol style="list-style-type: none"> 1. It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). 2. Excessive flux must be avoided. Please provide proper amount of flux. 3. When water-soluble flux is used sufficient washing is necessary. <p>5.2 Recommended soldering profile by various methods</p> <ol style="list-style-type: none"> 1. Soldering condition (Preheating temperature, soldering temperature and these times) is limited to reflow soldering method which is stipulated on the specification. 2. Chips should be mounted, shortly after solder is on a P.C. board. 3. Enough preheating is necessary to avoid chip cracking. Small temperature differences are less heat stress. 4. Temperature differences (ΔT) <p style="text-align: center;">Reflow soldering</p>  <p style="text-align: center;">Manual soldering (Solder iron)</p>  <p style="text-align: right;">* Temperature of metal cap surface Should not exceed 250°C.</p> <p>5.3 Recommended soldering peak temp and duration</p> <table border="1" data-bbox="544 1522 1209 1753"> <thead> <tr> <th rowspan="2" style="text-align: center;">Temp./Duration</th> <th colspan="2" style="text-align: center;">Reflow soldering</th> </tr> <tr> <th style="text-align: center;">Peak temp(°C)</th> <th style="text-align: center;">Duration(sec.)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Solder</td> <td></td> <td></td> </tr> <tr> <td style="text-align: center;">Sn-Pb Solder</td> <td style="text-align: center;">230 max.</td> <td style="text-align: center;">20 max.</td> </tr> <tr> <td style="text-align: center;">Lead Free Solder</td> <td style="text-align: center;">250 max.</td> <td style="text-align: center;">10 max.</td> </tr> </tbody> </table> <p>Recommended solder compositions</p> <p>Sn-37Pb (Sn-Pb solder)</p> <p>Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>	Temp./Duration	Reflow soldering		Peak temp(°C)	Duration(sec.)	Solder			Sn-Pb Solder	230 max.	20 max.	Lead Free Solder	250 max.	10 max.
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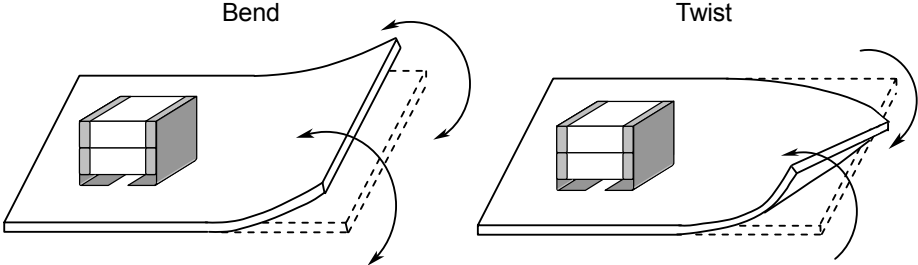
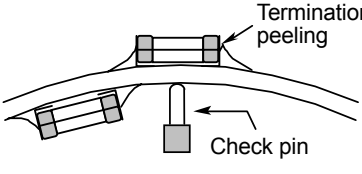
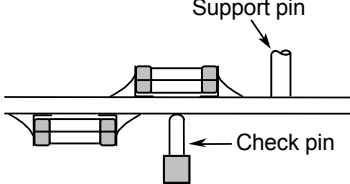
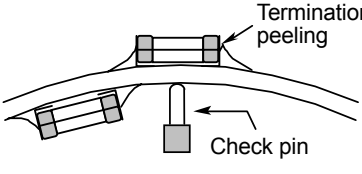
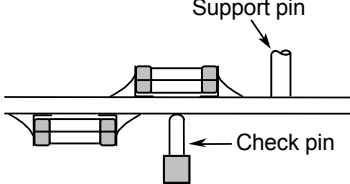
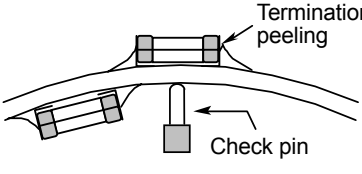
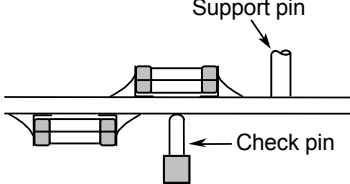
(12. Caution, continued)

No.	Process	Condition														
5	Soldering (continued)	<p>5.4 Avoiding thermal shock</p> <p>1. Preheating condition</p> <table border="1" data-bbox="581 239 989 390"> <thead> <tr> <th>Soldering</th> <th>Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td>Reflow soldering</td> <td>$\Delta T \leq 130$</td> </tr> <tr> <td>Manual soldering</td> <td>$\Delta T \leq 130$</td> </tr> </tbody> </table> <p>2. Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.</p> <p>5.5 Amount of solder</p> <p>Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.</p> <div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 30%;"> <p>Excessive solder</p>  </div> <div style="width: 35%; text-align: center;"> <p>Higher tensile force on the chip capacitor may cause cracking</p> </div> </div> <hr/> <div style="display: flex; justify-content: space-between; align-items: center;"> <div style="width: 30%;"> <p>Adequate</p>  </div> <div style="width: 35%; text-align: center;"> <p>Maximum amount Minimum amount</p> </div> </div> <hr/> <div style="display: flex; justify-content: space-between; align-items: flex-start;"> <div style="width: 30%;"> <p>Insufficient solder</p>  </div> <div style="width: 35%; text-align: center;"> <p>Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.</p> </div> </div> <hr/> <p>5.6 Solder repair by solder iron</p> <p>1. Selection of the soldering iron tip Tip temperature of solder iron varies by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation, however, heat shock may cause a crack in the chip capacitor. Please confirm the tip temperature before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)</p> <p style="text-align: center;">Recommended solder iron condition (Sn-Pb Solder and Lead Free Solder)</p> <table border="1" data-bbox="581 1520 1362 1621"> <thead> <tr> <th>Temp. (°C)</th> <th>Duration (sec.)</th> <th>Wattage (W)</th> <th>Shape (mm)</th> </tr> </thead> <tbody> <tr> <td>300 max.</td> <td>3 max.</td> <td>20 max.</td> <td>∅ 3.0 max.</td> </tr> </tbody> </table>	Soldering	Temp. (°C)	Reflow soldering	$\Delta T \leq 130$	Manual soldering	$\Delta T \leq 130$	Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	∅ 3.0 max.
Soldering	Temp. (°C)															
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300 max.	3 max.	20 max.	∅ 3.0 max.													

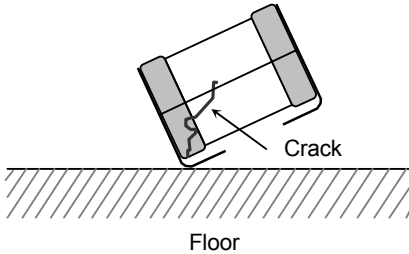
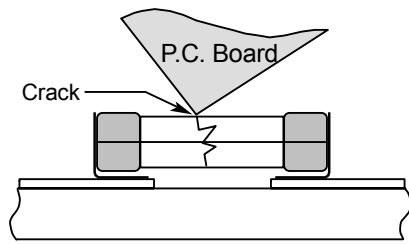
(12. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	<p>2. Direct contact of the soldering iron with ceramic dielectric of the chip capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5.7 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5.8 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially when the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex 1 "Recommendations to prevent the tombstone phenomenon")</p>
6	Cleaning (continued)	<p>1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and deteriorate the insulation resistance.</p> <p>2. If cleaning condition is not suitable, it may deteriorate the chip capacitor's insulation resistance.</p> <p>2.1 Insufficient washing</p> <ol style="list-style-type: none">1. Terminal electrodes may be corroded by Halogen in the flux.2. Halogen in the flux may adhere on the surface of capacitor, and lower the3 insulation resistance. <p>Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</p> <p>2.2 Excessive washing</p> <p>When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended.</p> <p style="text-align: center;">Power: 20 W/ℓmax. Frequency: 40 kHz max. Washing time: 5 minutes max.</p> <p>2.3 If the cleaning fluid is contaminated, of Halogen concentration can increases, and it may bring the same result as insufficient cleaning.</p>

(12. Caution, continued)

No.	Process	Condition						
7	Coating and molding of the P.C. Board	<ol style="list-style-type: none"> When the P.C. board is coated, please verify the impact on the capacitor. Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor. Please verify the curing temperature. 						
8	Handling after chip mounted	<ol style="list-style-type: none"> Please pay attention not to bend or distort the P.C. board after soldering otherwise the chip capacitor may crack. <div style="text-align: center; margin: 10px 0;">  </div> When functional check of the P.C. board is performed, higher pin pressure tends to be used for fear of loose contact. But if the pressure is excessive and bend the P.C. board, it may crack the chip capacitor or peel the termination. Please adjust the pins accordingly to ensure the P.C. board is not flexed. <table border="1" style="width: 100%; margin-top: 10px;"> <thead> <tr> <th data-bbox="526 1035 654 1087">Item</th> <th data-bbox="654 1035 1045 1087">Not recommended</th> <th data-bbox="1045 1035 1417 1087">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="526 1087 654 1367" style="vertical-align: middle;">Board bending</td> <td data-bbox="654 1087 1045 1367">  </td> <td data-bbox="1045 1087 1417 1367">  </td> </tr> </tbody> </table> 	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								

(12. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitors	<p>1. The chip capacitor may crack if dropped, especially large case sizes. Please handle with care and do not use if cracked.</p>  <p>2. When stacking the P.C. board for storage or handling, after soldering, the corner of the P.C. board may hit the chip capacitor of a neighboring board to cause crack.</p> 
10	Capacitance aging	Class 2 capacitors have aging characteristic, which is a decrease in capacitance over time due to crystalline changes that occur in ferroelectric ceramics. Careful consideration should be done in case of a time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life (and the estimated failure rate) depend on the temperature and voltage applied. This can be calculated by the equation described in JEITA RCR-2335B Annex 6) "Calculation of the estimated lifetime and the estimated failure rate". The risk can be decreased by reducing the temperature and voltage but it will not be guaranteed.
12	Others	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet:</p> <p>Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, Ships, etc.) Medical equipment. Power-generation control equipment. Atomic Energy-related equipment. Seabed equipment. Transportation control equipment. Public information-processing equipment. Military equipment. Electric heating Apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose Applications.</p> <p>When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup Circuits, etc., to ensure higher safety.</p>

11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example M 0 A - 00 - 000
 (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

12. TAPE PACKAGING SPECIFICATION

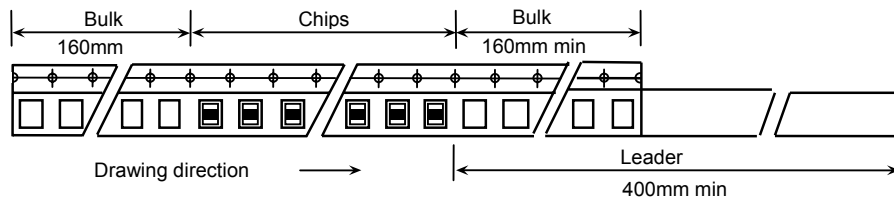
1. CONSTRUCTION AND DIMENSION OF TAPING

1. 1 Dimensions of carrier tape

Dimensions of paper tape shall be according to Appendix 3(CKG32K).

Dimensions of plastic tape shall be according to Appendix 4(CKG45K, CKG45N, CKG57K, CKG57N).

1. 2 Bulk part and leader of taping

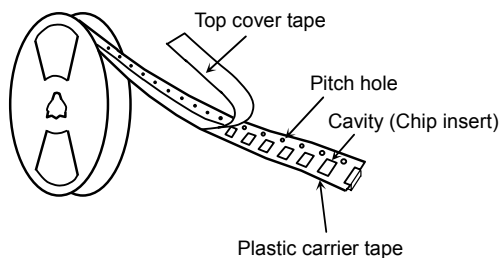


1.3 Dimensions of reel

Dimensions of $\varnothing 178$ reel shall be according to Appendix 5.

Dimensions of $\varnothing 330$ reel shall be according to Appendix 6.

1. 4 Structure of taping



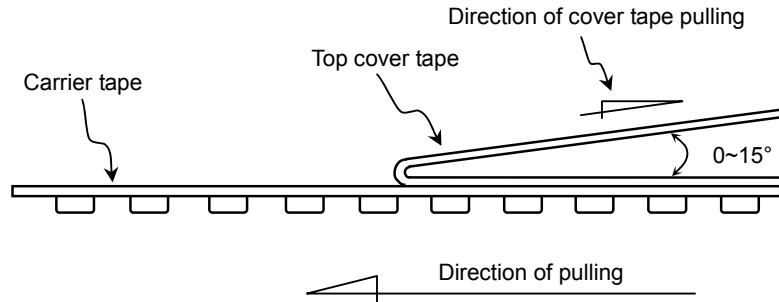
2. CHIP QUANTITY

Type	Taping Material	Chip quantity (pcs.)	
		$\varnothing 178$ mm reel	$\varnothing 330$ mm reel
CKG32K	plastic	1,000	4,000
CKG45K		————	1,000
CKG57K		————	1,000
CKG45N		————	1,000
CKG57N		————	1,000

3. PERFORMANCE SPECIFICATIONS

3. 1 Peel back cover (top tape)

0.05-0.7N. (See the following figure.)



3.2 Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.

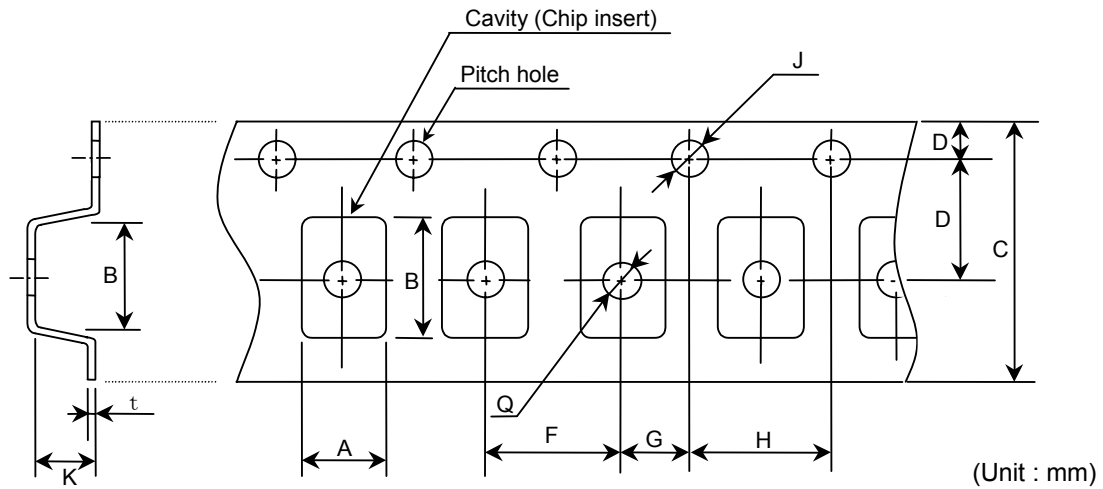
3. 3 The missing of components shall be less than 0.1%

3. 4 Components shall not stick to cover tape.

3. 5 The cover tapes shall not protrude beyond the edges of the carrier tape
Not shall cover the sprocket holes.

Appendix 3

Plastic Tape



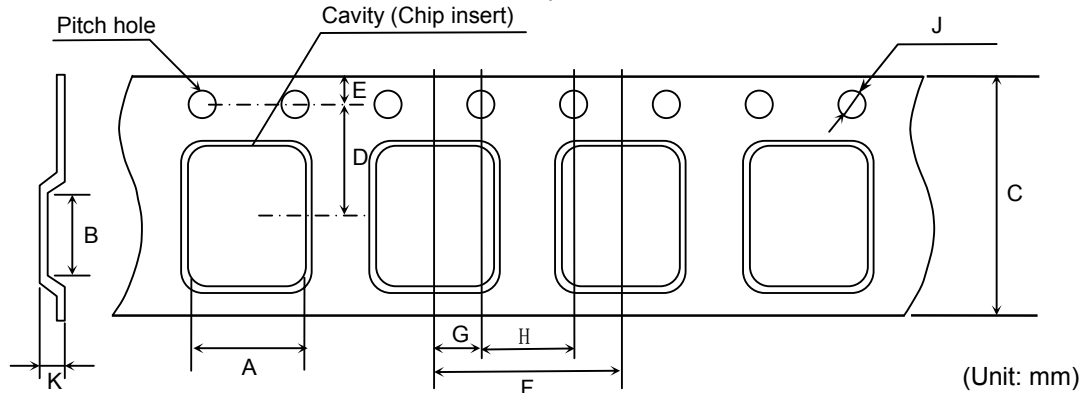
Symbol Type	A	B	C	D	E	F
CKG32K	(3.00)	(3.90)	12.0 ± 0.25	5.50 ± 0.05	1.75 ± 0.10	4.00 ± 0.10

Symbol Type	G	H	J	K	t	Q
CKG32K	2.00 ± 0.10	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	3.75 max.	0.50 ± 0.05	∅ 1.65 ± 0.10

* The values in the parentheses () are for reference.

Appendix 4

Plastic Tape



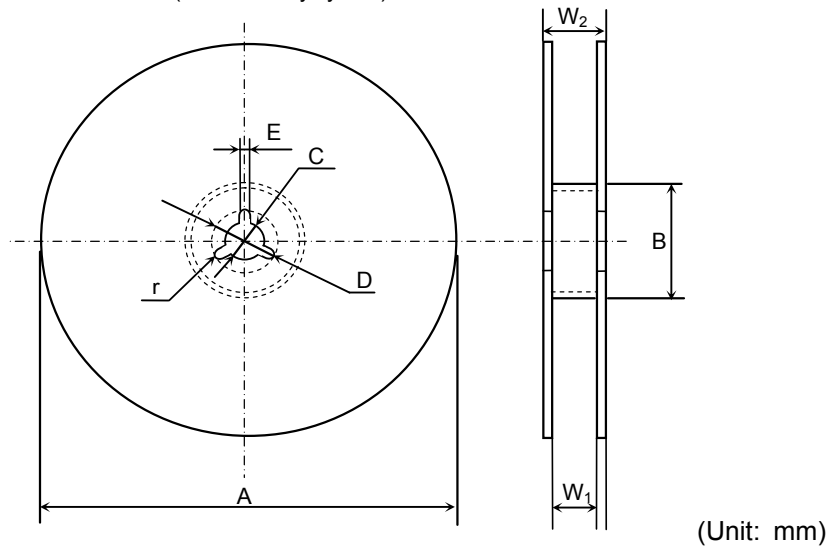
Symbol Type	A	B	C	D	E	F
CKG45K	(3.90)	(5.60)	12.0 ± 0.30	5.50 ± 0.10	1.75 ± 0.10	8.00 ± 0.10
CKG45N						
CKG57K	(5.60)	(6.60)	16.0 ± 0.30	7.50 ± 0.10	1.75 ± 0.10	8.00 ± 0.10
CKG57N						

Symbol Type	G	H	J	K
CKG45K	2.00 ± 0.10	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	3.75 max.
CKG45N				6.15 max.
CKG57K	2.00 ± 0.10	4.00 ± 0.10	∅ 1.5 ^{+0.10} ₀	4.15 max.
CKG57N				6.15 max.

* The values in the parentheses () are for reference.

Appendix 5

(Material: Polystyrene)

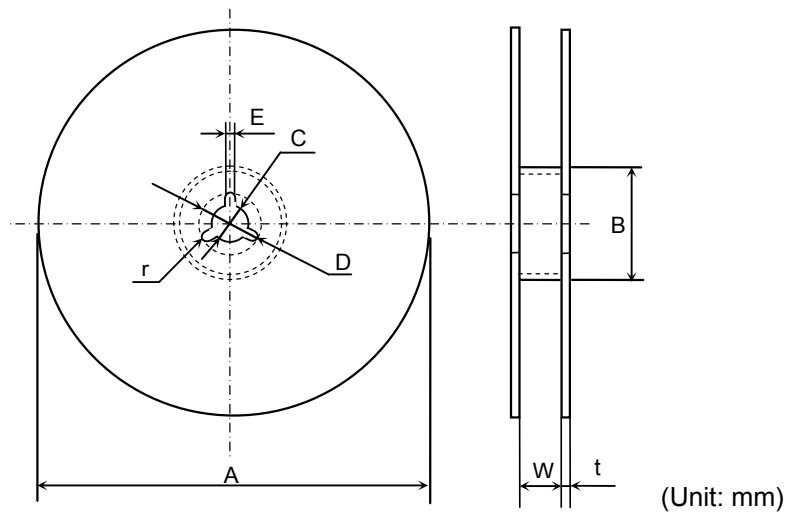


Symbol Dimension	A	B	C	D	E	W ₁
CKG32	Ø178 ± 2.0	Ø60 ± 2.0	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	13.0 ± 0.3

Symbol Dimension	W ₂	r
CKG32	17.0 ± 1.4	1.0

Appendix 6

(Material: Polystyrene)



Symbol Dimension	A	B	C	D	E	W
CKG32K	Ø382 max. (Nominal Ø330)	Ø50 min.	Ø13 ± 0.5	Ø21 ± 0.8	2.0 ± 0.5	14.0 ± 1.5
CKG45K, CKG45N						13.5 ± 1.5
CKG57K, CKG57N						17.5 ± 1.5

Symbol Dimension	t	r
CKG32	2.0 ± 0.5	1.0
CKG45K, CKG45N		
CKG57K, CKG57N		

END PAGE