



SPECIFICATION

SPEC. No. _____

DATE : _____

CUSTOMER'S PRODUCT NAME	TDK PRODUCT NAME CLLC1A, CLLE1A Series
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Please sign and return this specification to your local TDK representatives. If orders are placed without this returned documentation, we must consider you found the specification acceptable.

THIS SPECIFICATION IS RECEIVED

DATE: _____ YEAR _____ MONTH _____ DAY _____

TDK-EPC Corporation
1-13-1, Nihonbashi, Chuo-ku, Tokyo
103-0027, Japan

ENGINEERING

ISSUED	CHECKED	APPROVED
DATE	DATE	DATE

Sales Office _____

Sales Tel. () _____

PRODUCT CLASSIFICATION CODE	040320
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1. SCOPE

This specification is applicable to chip type multilayer ceramic capacitors with a priority over other relevant specifications. Production places defined in this specification shall be TDK-EPC Corporation Japan, TDK (Suzhou) Co., Ltd, TDK-EPC HONG KONG LIMITED, TDK (Malaysia) Sdn. Bhd, and TDK Components U.S.A. Inc.

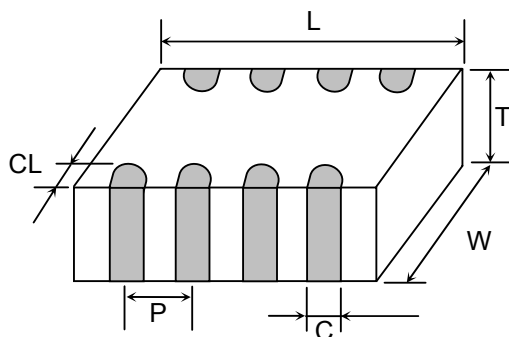
EXPLANATORY NOTE:

This specification warrants the quality of the TDK ceramic chip capacitors. The product should be evaluated and confirmed in your product before use. If the use of the product exceeds the bounds of this specification, we can not guarantee its quality and reliability.

2. CODE CONSTRUCTION

(Example)	<u>CLLC1A</u>	<u>X7S</u>	<u>0G</u>	<u>105</u>	<u>M</u>	<u>T</u>
	<u>CLLE1A</u>	<u>X7S</u>	<u>0G</u>	<u>475</u>	<u>M</u>	<u>T</u>
	(1)	(2)	(3)	(4)	(5)	(6)

1. Type



Please refer to product list for the dimension of each product. See Section 8 for inside structure and material.

2. Temperature Characteristics (Details are shown in Section 7, No.6)

3. Rated Voltage

Symbol	Rated Voltage
1A	DC 10 V
0J	DC 6.3 V
0G	DC 4 V

4. Rated Capacitance

Stated in three digits and in units of pico farads (pF).

The first and second digits identify the first and second significant figures of the capacitance; the third digit identifies the multiplier.

R is designated for a decimal point.

Example 105 → 1,000,000pF

5. Capacitance tolerance

Symbol	Tolerance
M	± 20 %

6. Packaging

Symbol	Packaging
B	Bulk
T	Taping

3. RATED CAPACITANCE AND CAPACITANCE TOLERANCE

1. Standard combination of rated capacitance and tolerances

Temperature Characteristics	Capacitance tolerance	Rated capacitance
X7R X7S	M (± 20 %)	E – 6 series

2. Capacitance Step in E series

E series	Capacitance Step					
E- 6	1.0	1.5	2.2	3.3	4.7	6.8

4. OPERATING TEMPERATURE RANGE

T.C.	Min. operating Temperature	Max. operating Temperature	Reference Temperature
X7R X7S	-55°C	125°C	25°C

5. STORING CONDITION AND TERM

5 to 40°C at 20 to 70%RH
6 months Max.

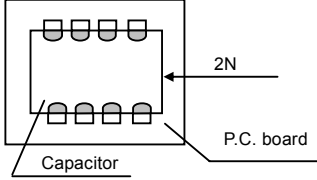
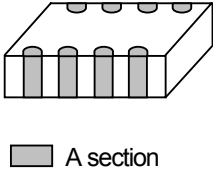
6. INDUSTRIAL WASTE DISPOSAL

Dispose this product as industrial waste in accordance with the local Industrial Waste Laws.

7. PERFORMANCE

No.	Item	Performance	Test or inspection method														
1	External Appearance	No defects which may affect performance.	Inspect with magnifying glass. (3X magnifications)														
2	Insulation Resistance	100MΩ·μF min.	Apply rated voltage for 60s. Measure 8 terminal electrodes at the same time.														
3	Voltage Proof	Withstand test voltage without insulation breakdown or other damage.	2.5 times of rated voltage Above DC voltage shall be applied for 1~5s. Charge / discharge current shall not exceed 50mA. Measure 8 terminal electrodes at the same time.														
4	Capacitance	Within the specified tolerance at 1000hrs age (Per IEC-384-9).	<table border="1"> <thead> <tr> <th>Measuring frequency</th> <th>WV</th> <th>Measuring voltage</th> </tr> </thead> <tbody> <tr> <td rowspan="2">1kHz±10%</td> <td>10V</td> <td>1.0±0.2Vrms.</td> </tr> <tr> <td>6.3V and under</td> <td>0.5±0.2Vrms.</td> </tr> </tbody> </table> <p>Measure 8 terminal electrodes at the same time.</p>	Measuring frequency	WV	Measuring voltage	1kHz±10%	10V	1.0±0.2Vrms.	6.3V and under	0.5±0.2Vrms.						
Measuring frequency	WV	Measuring voltage															
1kHz±10%	10V	1.0±0.2Vrms.															
	6.3V and under	0.5±0.2Vrms.															
5	Dissipation Factor	<table border="1"> <thead> <tr> <th colspan="2">Characteristics</th> </tr> <tr> <th>T.C.</th> <th>D.F.</th> </tr> </thead> <tbody> <tr> <td>X7R</td> <td rowspan="2">0.10 max.</td> </tr> <tr> <td>X7S</td> </tr> </tbody> </table>	Characteristics		T.C.	D.F.	X7R	0.10 max.	X7S	See No.4 in this table for measuring condition.							
Characteristics																	
T.C.	D.F.																
X7R	0.10 max.																
X7S																	
6	Temperature Characteristics of Capacitance	<table border="1"> <thead> <tr> <th>Capacitance Change (%)</th> </tr> <tr> <th>No DC voltage applied</th> </tr> </thead> <tbody> <tr> <td>X7R : ±15</td> </tr> <tr> <td>X7S : ±22</td> </tr> </tbody> </table>	Capacitance Change (%)	No DC voltage applied	X7R : ±15	X7S : ±22	<p>Capacitance shall be measured by the steps shown in the following table after thermal equilibrium is obtained for each step.</p> <p>Capacitance change shall be calculated by the value of the reference temperature in Step 3.</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temperature(°C)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>25 ± 2</td> </tr> <tr> <td>2</td> <td>-55 ± 2</td> </tr> <tr> <td>3</td> <td>25 ± 2</td> </tr> <tr> <td>4</td> <td>125 ± 2</td> </tr> </tbody> </table>	Step	Temperature(°C)	1	25 ± 2	2	-55 ± 2	3	25 ± 2	4	125 ± 2
Capacitance Change (%)																	
No DC voltage applied																	
X7R : ±15																	
X7S : ±22																	
Step	Temperature(°C)																
1	25 ± 2																
2	-55 ± 2																
3	25 ± 2																
4	125 ± 2																

(7. Performance, continued)

No.	Item	Performance	Test or inspection method					
7	Robustness of Terminations	No sign of termination coming off, breakage of ceramic, or other abnormal signs.	Reflow solder the capacitors on P.C. board (shown in Appendix 1 and 2) and apply a pushing force of for 10 ± 1 s. 					
8	Solderability	All terminations shall exhibit a continuous solder coating free from defects for a minimum of 75% of the surface area of any individual termination. Anomalies other than dewetting, non-wetting, and pin holes are not cause for rejection. 	Completely soak both terminations in solder at $235 \pm 5^\circ\text{C}$ for 2 ± 0.5 s. Solder : H63A (JIS Z 3282) Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.					
9	Resistance to solder heat	External appearance	No cracks are allowed and terminations shall be covered at least 60% with new solder.					
		Capacitance	<table border="1" data-bbox="591 1220 938 1377"> <thead> <tr> <th data-bbox="591 1220 753 1297">Characteristics</th> <th data-bbox="753 1220 938 1297">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="591 1297 753 1335">X7R</td> <td data-bbox="753 1297 938 1335" rowspan="2" style="text-align: center;">$\pm 7.5\%$</td> </tr> <tr> <td data-bbox="591 1335 753 1377">X7S</td> </tr> </tbody> </table>	Characteristics	Change from the value before test	X7R	$\pm 7.5\%$	X7S
	Characteristics	Change from the value before test						
	X7R	$\pm 7.5\%$						
X7S								
	D.F.	Meet the initial spec.	Preheating condition Temp. : $150 \pm 10^\circ\text{C}$ Time : 1 to 2min. Flux : Isopropyl alcohol (JIS K 8839) Rosin (JIS K 5902) 25% solid solution.					
	Insulation Resistance	Meet the initial spec.	Solder : H63A (JIS Z 3282) Leave the capacitor in ambient conditions for 24 ± 2 h before measurement.					

(7. Performance, continued)

No.	Item		Performance	Test or inspection method	
12	Moisture Resistance (Steady State)	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1 and 2) before testing. Leave at temperature $40 \pm 2^{\circ}\text{C}$, 90 to 95%RH for 500 +24,0h. Leave the specimen in ambient conditions for $24 \pm 2\text{h}$ before the measurement.	
		Capacitance	Characteristics		Change from the value before test
			X7R X7S		$\pm 12.5 \%$
		D.F.	Characteristics X7R/X7S : 200% of initial spec. max.		
Insulation Resistance	10M Ω · μF min.				
13	Moisture Resistance	External appearance	No mechanical damage.	Reflow solder the capacitor on P.C. board (shown in Appendix 1 and 2) before testing. Apply the rated voltage at temperature $40 \pm 2^{\circ}\text{C}$, and 90 to 95%RH for 500+24,0h Charge/discharge current shall not exceed 50mA. Leave the capacitor in ambient conditions for $48 \pm 4\text{h}$ before measurement. Voltage conditioning: Voltage treats the specimen under testing temperature and voltage for 1 hour. Leave the capacitor in ambient conditions for $24 \pm 2\text{h}$ before measurement. Use this measurement for initial value.	
		Capacitance	Characteristics		Change from the value before test
			X7R X7S		$\pm 12.5 \%$
		D.F.	Characteristics X7R/X7S : 200% of initial spec. max.		
Insulation Resistance	5M Ω · μF min.				

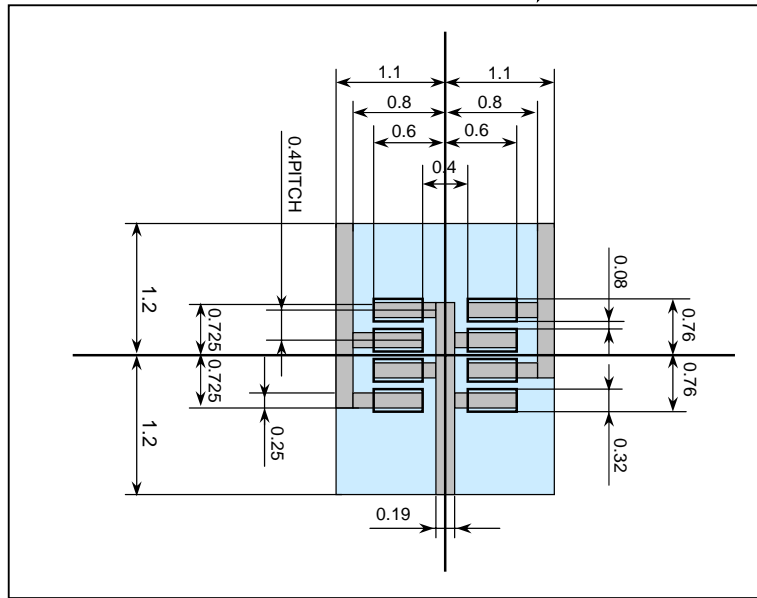
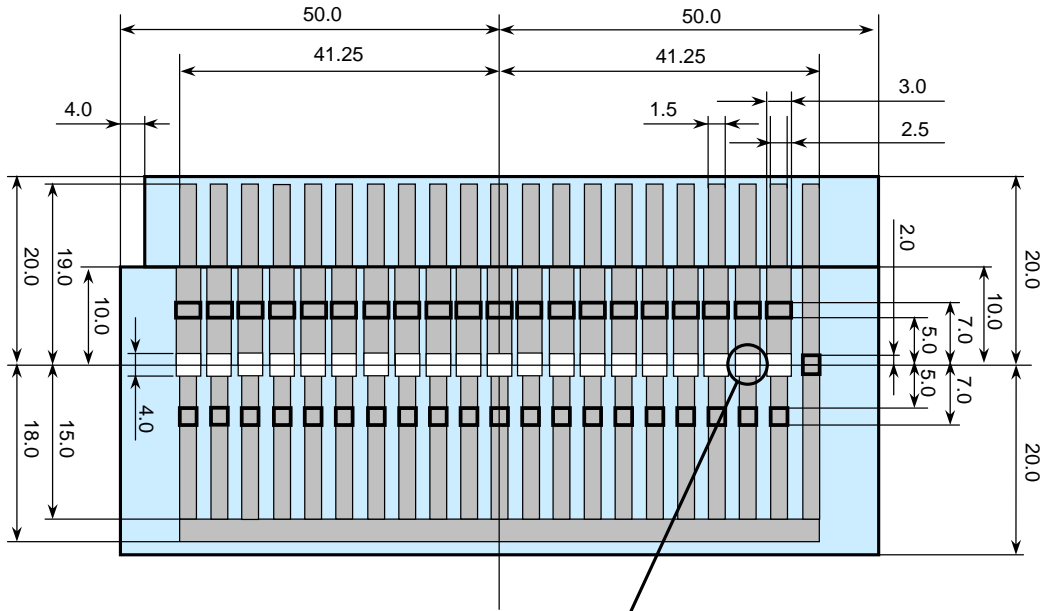
(7. Performance, continued)

No.	Item	Performance	Test or inspection method					
14	Life	External appearance	No mechanical damage.					
	Capacitance	<table border="1" data-bbox="597 300 938 457"> <thead> <tr> <th data-bbox="597 300 760 363">Characteristics</th> <th data-bbox="760 300 938 363">Change from the value before test</th> </tr> </thead> <tbody> <tr> <td data-bbox="597 363 760 426">X7R</td> <td data-bbox="760 363 938 426" rowspan="2">± 15 %</td> </tr> <tr> <td data-bbox="597 426 760 457">X7S</td> </tr> </tbody> </table>	Characteristics	Change from the value before test	X7R	± 15 %	X7S	<p>Reflow solder the capacitor on P.C. board (shown in Appendix 1 and 2) before testing.</p> <p>Apply the rated voltage at 125±2°C for 1,000 +48,0h</p> <p>Charge/discharge current shall not exceed 50mA.</p>
	Characteristics	Change from the value before test						
	X7R	± 15 %						
X7S								
D.F.	<p>Characteristics</p> <p>X7R/X7S :</p> <p>200% of initial spec. max.</p>	<p>Leave the specimen in ambient conditions for 24±2h before measurement.</p>						
Insulation Resistance	10MΩ·μF min.	<p>Voltage conditioning:</p> <p>Voltage treats the capacitor under testing temperature and voltage for 1 hour.</p> <p>Leave the specimen in ambient conditions for 48±4h before measurement as initial value.</p>						

Appendix 1

CLLC1A

PC Board



(Unit: mm)

1. Material: Glass Epoxy (As per JIS C6484 GE4)

2. Thickness: 0.8mm

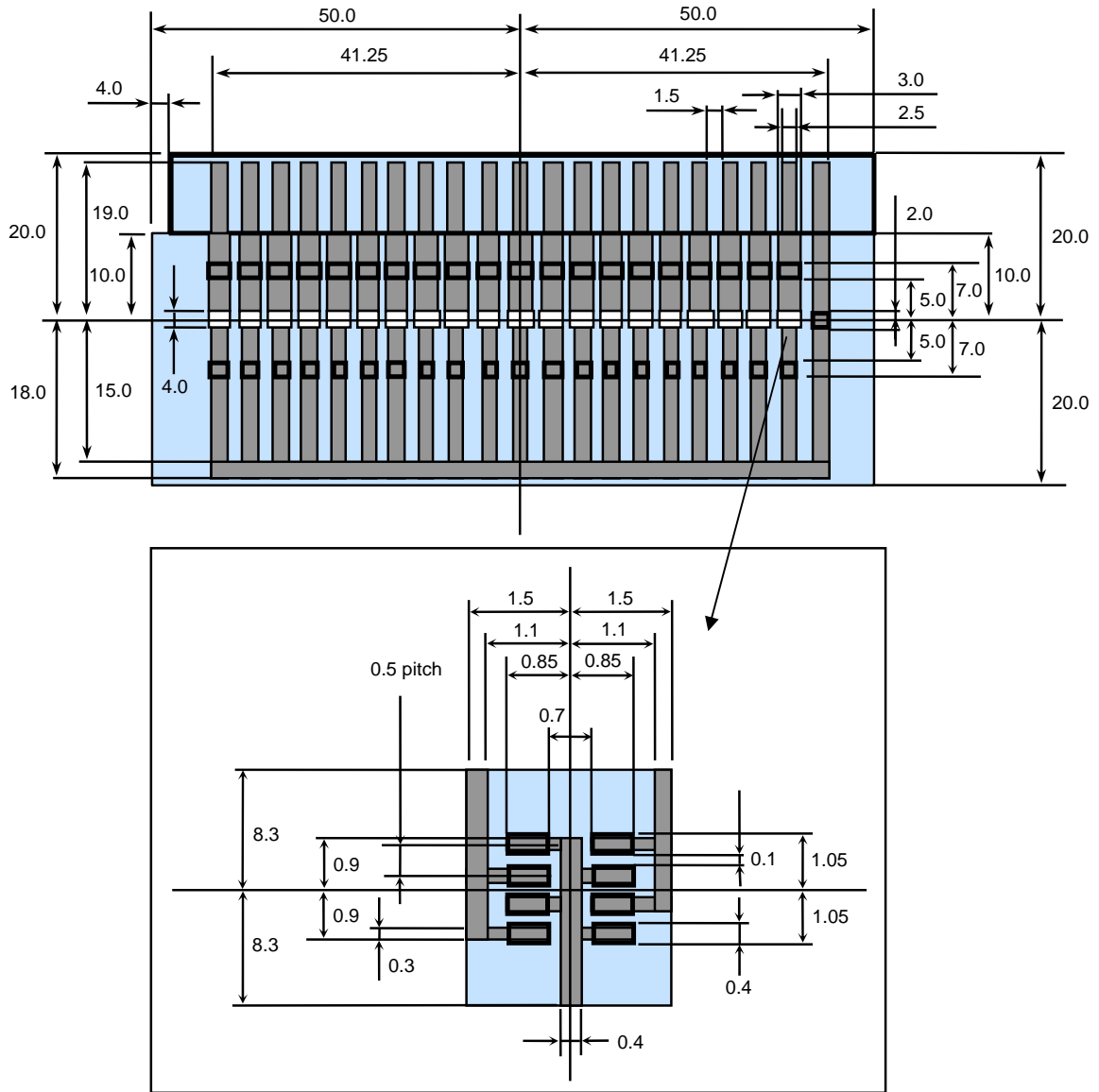
 Copper (Thickness: 0.035mm)

 Solder resist

Appendix 2

CLLE1A

PC Board



(Unit: mm)

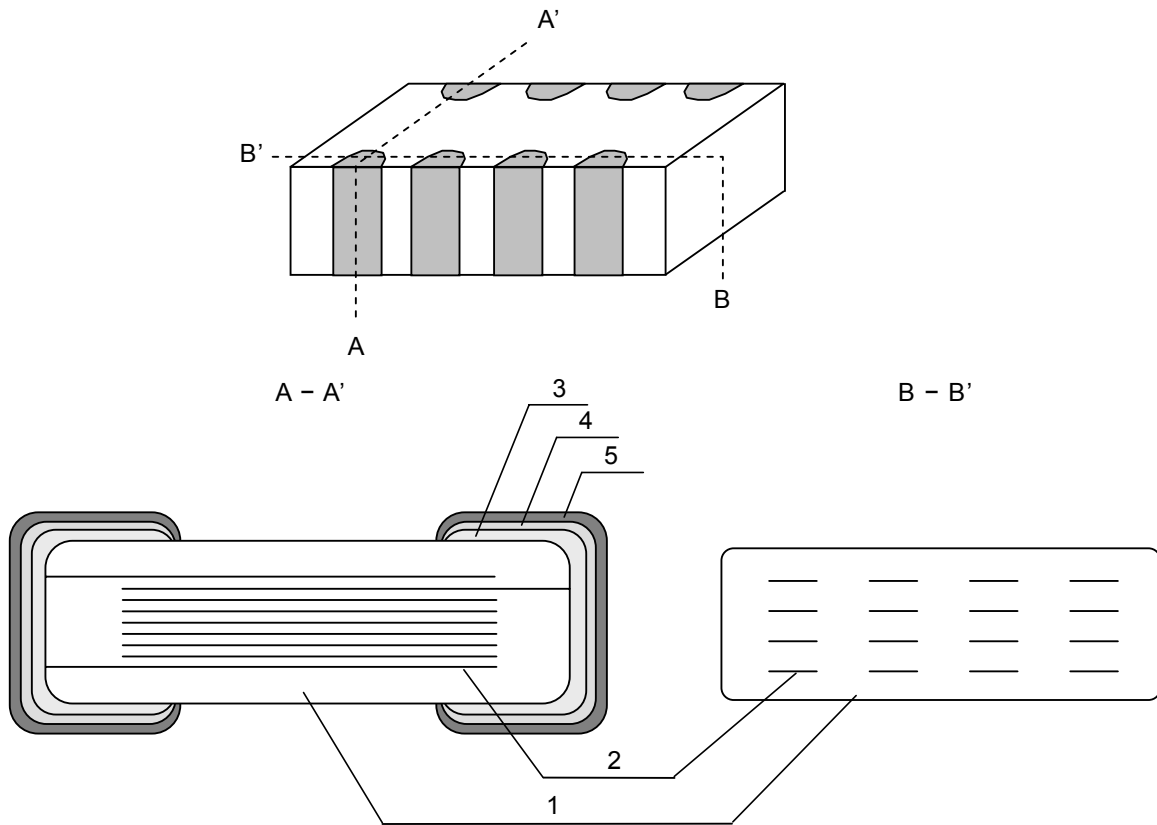
1. Material: Glass Epoxy (As per JIS C6484 GE4)

2. Thickness: 1.6mm

 Copper (Thickness: 0.035mm)

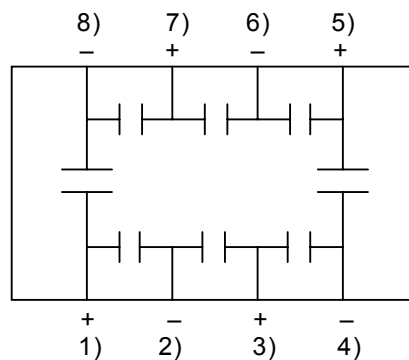
 Solder resist

8. INSIDE STRUCTURE AND MATERIAL



No.	NAME	MATERIAL
1	Dielectric	BaTiO ₃
2	Electrode	Ni
3	Termination	Cu
4		Ni
5		Sn

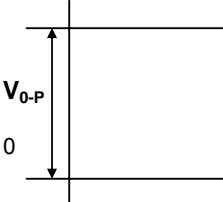
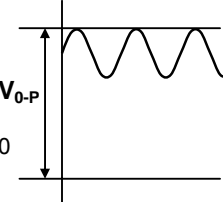
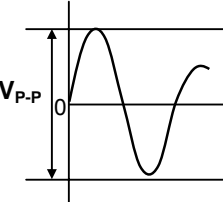
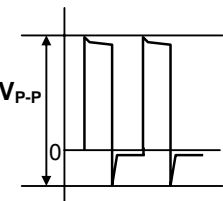
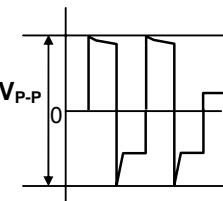
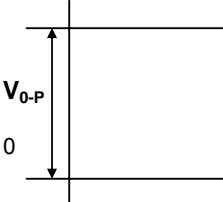
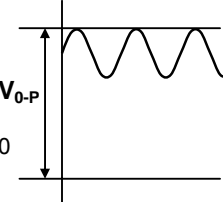
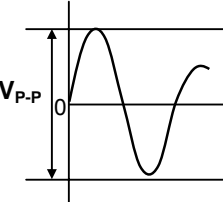
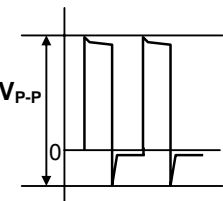
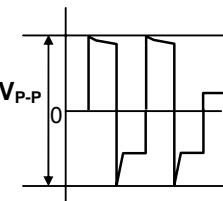
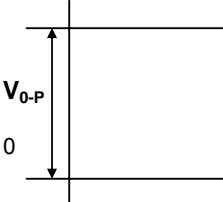
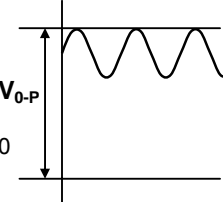
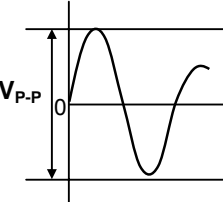
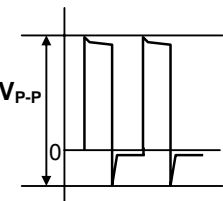
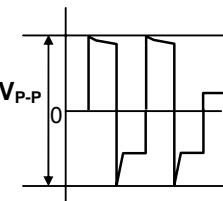
9. EQUIVALENT CIRCUIT



+ 1) 3) 5) 7)
- 2) 4) 6) 8)

8 terminals are connected and measured at the same time.

12. Caution

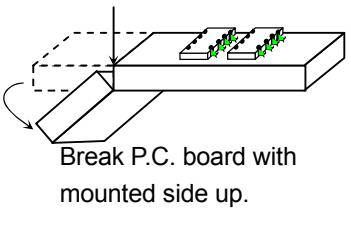
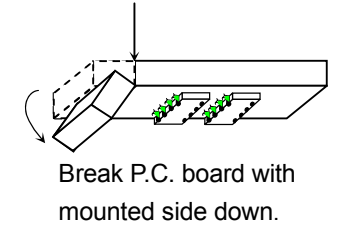
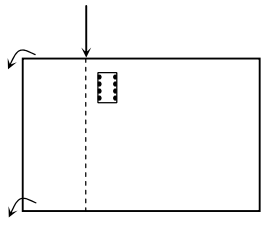
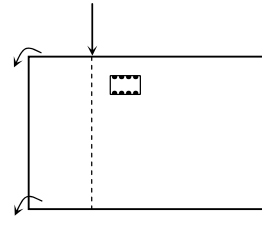
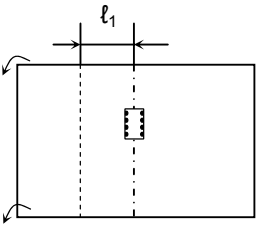
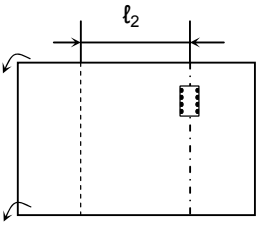
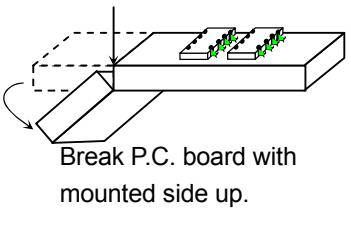
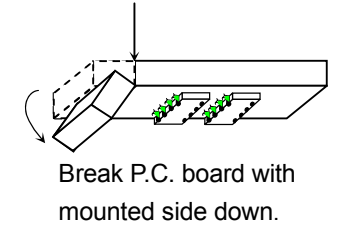
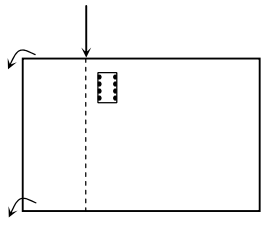
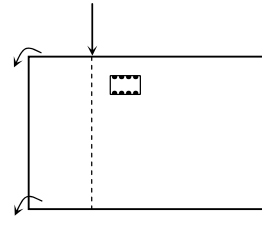
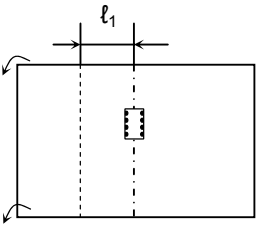
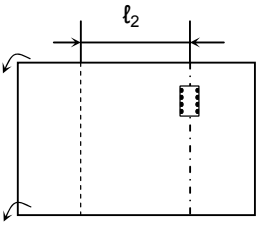
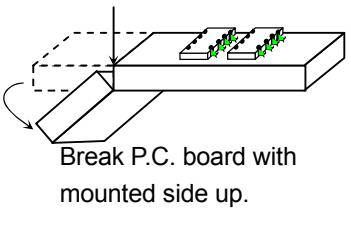
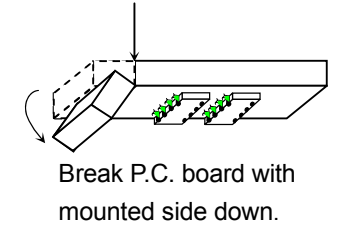
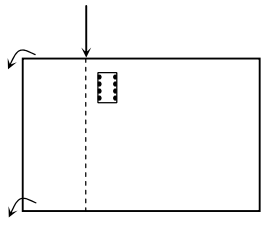
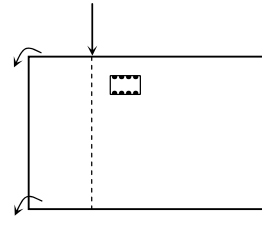
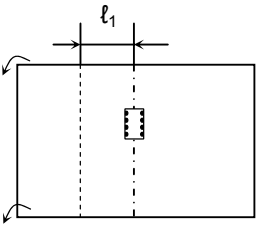
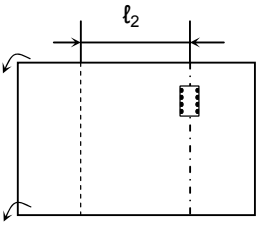
No.	Process	Condition																
	Operating Condition (Storage, Transportation)	<p>1.1 Storage</p> <ol style="list-style-type: none"> The capacitor must be stored in an ambient temperature of 5 to 40°C with a relative humidity of 20 to 70%RH. The product should be used within 6 months upon receipt. The capacitor must be operated and stored in an environment free of condensation and corrosive gases such as hydrogen sulphide, hydrogen sulphate, chlorine, ammonia and sulfur. Avoid storing in sun light and falling of dew. Do not use capacitor under high humidity and high/low atmospheric pressure which may compromise product reliability. Capacitor should be tested for solderability when stored for long periods of time. <p>1.2 Handling in transportation In case of the transportation, the performance of the capacitor may be deteriorated depending on the transportation condition. (Refer to JEITA RCR-2335B 9.2 "Handling in transportation")</p>																
2	Circuit design	<p>2.1 Operating temperature Operating temperature should be followed strictly within this specification.</p> <ol style="list-style-type: none"> Do not use capacitors above the maximum allowable operating temperature. Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitors will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the product it's mounted on. Please design the circuit so that the maximum temperature of the capacitors (including the self heating) will be below the maximum allowable operating temperature. Temperature rise at capacitor surface shall be below 20°C) The electrical characteristics of the capacitor will vary depending on the temperature. The capacitor should be selected and designed after taking temperature into consideration. <p>2.2 Operating voltage</p> <ol style="list-style-type: none"> Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, V_{0-P} must be below the rated voltage. (Reference figures 1 and 2 below). AC or pulse with overshooting, V_{P-P} must be below the rated voltage. (Reference figures 3, 4, and 5 below). When the voltage is started/stopped to the circuit an irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use the capacitor within rated voltage during these Irregular voltage periods. <table border="1" data-bbox="500 1297 1409 1820"> <thead> <tr> <th data-bbox="500 1297 678 1337">Voltage</th> <th data-bbox="678 1297 922 1337">(1) DC voltage</th> <th data-bbox="922 1297 1166 1337">(2) DC+AC voltage</th> <th data-bbox="1166 1297 1409 1337">(3) AC voltage</th> </tr> </thead> <tbody> <tr> <td data-bbox="500 1337 678 1549">Positional Measurement (Rated voltage)</td> <td data-bbox="678 1337 922 1549">  </td> <td data-bbox="922 1337 1166 1549">  </td> <td data-bbox="1166 1337 1409 1549">  </td> </tr> <tr> <th data-bbox="500 1570 678 1610">Voltage</th> <th data-bbox="678 1570 922 1610">(4) Pulse voltage (A)</th> <th data-bbox="922 1570 1166 1610">(5) Pulse voltage (B)</th> <th></th> </tr> <tr> <td data-bbox="500 1610 678 1820">Positional Measurement (Rated voltage)</td> <td data-bbox="678 1610 922 1820">  </td> <td data-bbox="922 1610 1166 1820">  </td> <td></td> </tr> </tbody> </table>	Voltage	(1) DC voltage	(2) DC+AC voltage	(3) AC voltage	Positional Measurement (Rated voltage)				Voltage	(4) Pulse voltage (A)	(5) Pulse voltage (B)		Positional Measurement (Rated voltage)			
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(10. Caution, continued)

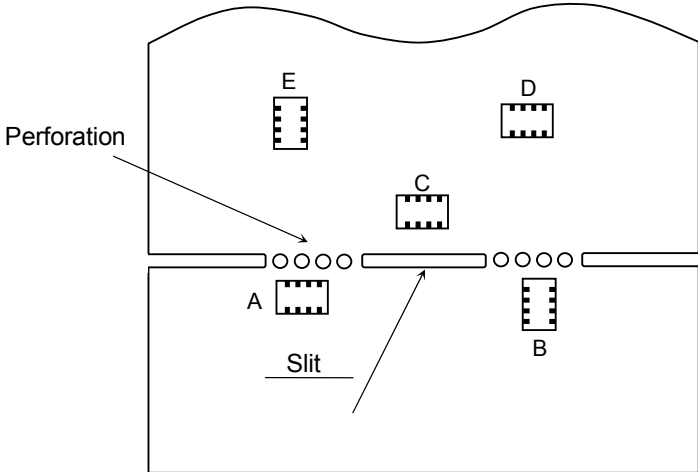
No.	Process	Condition
2	Circuit design (continued)	<p>2.2 Operating Voltage (continued)</p> <p>2. Even below the rated voltage, if repetitive high AC frequency or pulsed voltage is applied, the reliability of the capacitors may be reduced.</p> <p>3. The effective capacitance will vary depending on applied DC and AC voltages. The capacitor should be selected after considering the voltage affect.</p> <p>2.3 Frequency</p> <p>When Class 2 capacitors are used in AC and/or pulsed voltages, the capacitor may self vibrate and generate audible sound (piezoelectric affect).</p>

3	Designing P.C. Board	<p>The amount of solder at the terminations has a direct effect on the reliability of the capacitors.</p> <ol style="list-style-type: none"> 1. The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder lands to have proper amount of solder on the terminations. 2. Avoid using common solder land for multiple terminations and provide individual solder land for each termination instead. 3. Size and recommended land dimensions provided below: <div style="text-align: center;"> </div> <p style="text-align: center;">Recommended Land Dimensions (mm)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Type Symbol</th> <th>CLLC1A (CC0603)</th> <th>CLLE1A (CC0805)</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>0.25</td> <td>0.3</td> </tr> <tr> <td>B</td> <td>0.4</td> <td>0.3 ~ 0.6</td> </tr> <tr> <td>C</td> <td>1.2</td> <td>1.3 ~ 1.8</td> </tr> <tr> <td>D</td> <td>0.4</td> <td>0.5 ~ 0.8</td> </tr> <tr> <td>P</td> <td>0.4</td> <td>0.5</td> </tr> </tbody> </table>	Type Symbol	CLLC1A (CC0603)	CLLE1A (CC0805)	A	0.25	0.3	B	0.4	0.3 ~ 0.6	C	1.2	1.3 ~ 1.8	D	0.4	0.5 ~ 0.8	P	0.4	0.5
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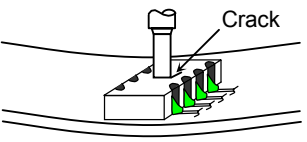
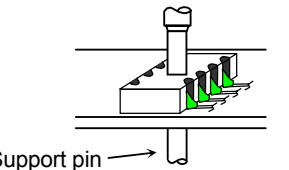
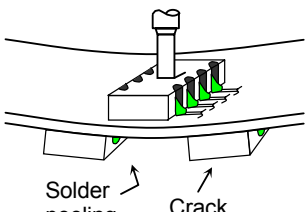
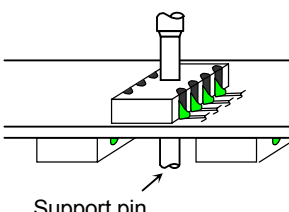
(10. Caution, continued)

No.	Process	Condition												
3	Designing P.C. board (continued)	<p>4. Recommended chip capacitor layout is provided below:</p> <table border="1"> <thead> <tr> <th data-bbox="509 268 672 344"></th> <th data-bbox="672 268 1032 344">Disadvantage against bending stress</th> <th data-bbox="1032 268 1393 344">Advantage against bending stress</th> </tr> </thead> <tbody> <tr> <td data-bbox="509 344 672 737">Mounting face</td> <td data-bbox="672 344 1032 737"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p> </td> <td data-bbox="1032 344 1393 737"> <p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p> </td> </tr> <tr> <td data-bbox="509 737 672 1157">Chip arrangement (Direction)</td> <td data-bbox="672 737 1032 1157"> <p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p>  </td> <td data-bbox="1032 737 1393 1157"> <p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p>  </td> </tr> <tr> <td data-bbox="509 1157 672 1604">Distance from slit</td> <td data-bbox="672 1157 1032 1604"> <p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p> </td> <td data-bbox="1032 1157 1393 1604"> <p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p> </td> </tr> </tbody> </table>		Disadvantage against bending stress	Advantage against bending stress	Mounting face	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side up.</p>	<p>Perforation or slit</p>  <p>Break P.C. board with mounted side down.</p>	Chip arrangement (Direction)	<p>Mount perpendicularly to perforation or slit</p> <p>Perforation or slit</p> 	<p>Mount in parallel with perforation or slit</p> <p>Perforation or slit</p> 	Distance from slit	<p>Closer to slit is higher stress</p>  <p>$(l_1 < l_2)$</p>	<p>Away from slit is less stress</p>  <p>$(l_1 < l_2)$</p>
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(10. Caution, continued)

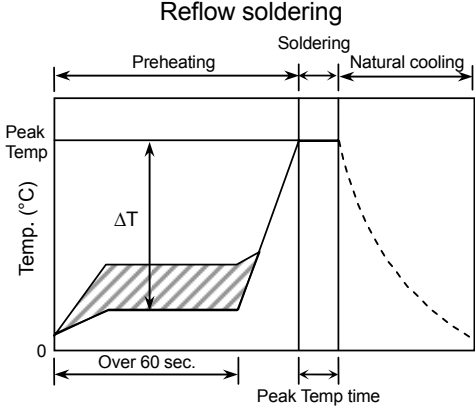
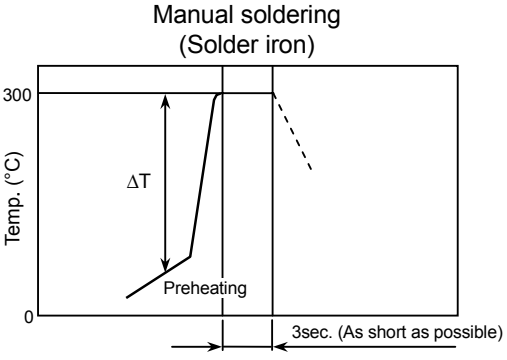
No.	Process	Condition
3	Designing P.C. board (continued)	<p>5. Mechanical stress varies according to location of chip capacitor on the P.C. board.</p>  <p>The relative stress applied to these capacitors during depaneling is in the following order:</p> $A > B = C > D > E$

4	Mounting	<p>4.1 Stress from mounting head</p> <p>If the mounting head is adjusted too low, it may induce excessive stress on the chip capacitors and result in cracking. Please take following precautions:</p> <ol style="list-style-type: none"> 1. Adjust the bottom dead center of the mounting head to reach the P.C. board surface and but not contact it. 2. Adjust the mounting head pressure to be 1 to 3N of static weight. 3. To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board. See following examples.
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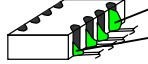
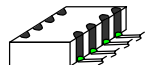

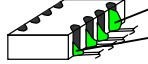
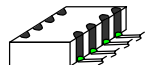

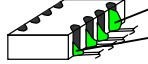
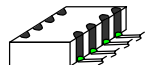
	Not recommended	Recommended
Single sided mounting		
Double-sides mounting		

When the centering jaw is worn, mechanical impact on the capacitor may occur and damage the product. Please control the closing dimension of the centering jaw and provide sufficient preventive maintenance and/or replacement if necessary.

(10. Caution, continued)

No.	Process	Condition									
5	Soldering	<p>5.1 Flux selection</p> <p>Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitor. To avoid such degradation, the following is recommended.</p> <ol style="list-style-type: none"> 1. It is recommended to use a mildly activated rosin flux (less than 0.1wt% chlorine). 2. Excessive flux must be avoided. Please provide proper amount of flux. 3. When water-soluble flux is used, sufficient washing is necessary. <p>5.2 Recommended soldering profile by various methods</p> <div style="text-align: center;"> <p>Reflow soldering</p>  <p>The graph shows temperature in degrees Celsius on the y-axis. The x-axis is divided into three phases: Preheating (duration: Over 60 sec.), Soldering (duration: Peak Temp time), and Natural cooling. The temperature rises during preheating, reaches a peak during soldering, and then cools naturally. A shaded area under the preheating curve is labeled ΔT.</p> </div> <div style="text-align: center;"> <p>Manual soldering (Solder iron)</p>  <p>The graph shows temperature in degrees Celsius on the y-axis, with a mark at 300. The x-axis shows Preheating and Soldering phases. The temperature rises during preheating, reaches a peak during soldering, and then cools. A shaded area under the preheating curve is labeled ΔT. The soldering phase duration is marked as 3sec. (As short as possible).</p> </div> <p>5.3 Recommended soldering peak temp and duration</p> <table border="1" data-bbox="584 1470 1242 1648"> <thead> <tr> <th></th> <th>Peak temp</th> <th>Duration</th> </tr> </thead> <tbody> <tr> <td>Pb-Sn Solder</td> <td>230°C max.</td> <td>20 sec. max.</td> </tr> <tr> <td>Lead Free Solder</td> <td>260°C max.</td> <td>10 sec. max.</td> </tr> </tbody> </table> <p>Recommended solder compositions Sn-37Pb (Pb-Sn solder) Sn-3.0Ag-0.5Cu (Lead Free Solder)</p>		Peak temp	Duration	Pb-Sn Solder	230°C max.	20 sec. max.	Lead Free Solder	260°C max.	10 sec. max.
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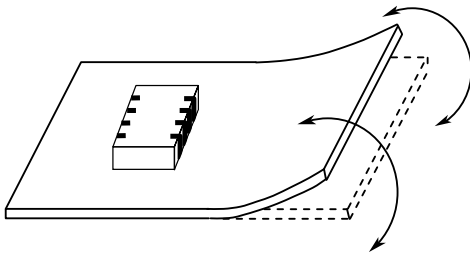
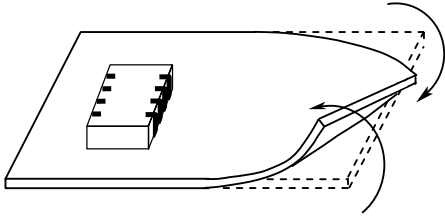
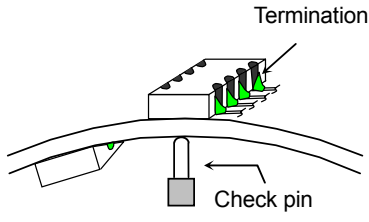
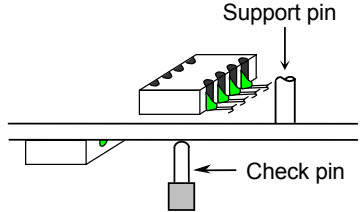
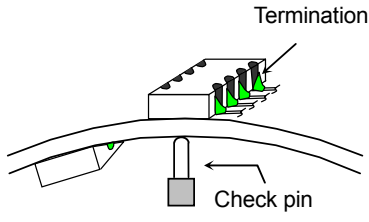
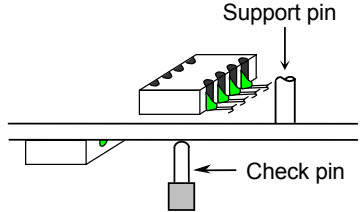
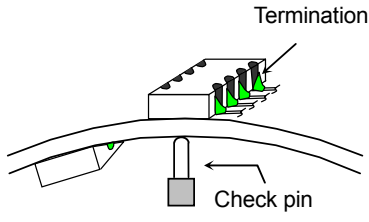
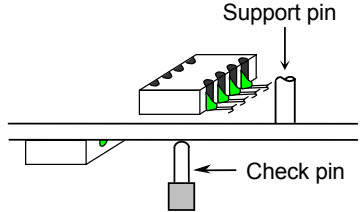
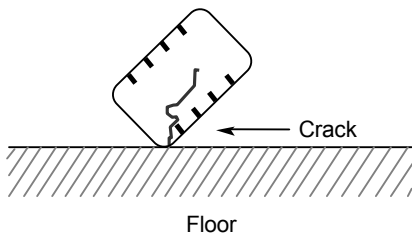
(10. Caution, continued)

No.	Process	Condition																											
5	Soldering (continued)	<p>5.4 Avoiding thermal shock</p> <p>1. Preheating condition</p> <table border="1" data-bbox="610 233 1149 388"> <thead> <tr> <th>Soldering</th> <th>Temp. (°C)</th> </tr> </thead> <tbody> <tr> <td>Reflow soldering</td> <td>$\Delta T \leq 150$</td> </tr> <tr> <td>Manual soldering</td> <td>$\Delta T \leq 150$</td> </tr> </tbody> </table> <p>2. Cooling condition Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100°C.</p> <p>5.5 Amount of solder Excessive solder will induce higher tensile force on the chip capacitor during temperature changes and may result in chip cracking. In sufficient solder may detach the capacitor from the P.C. board.</p> <p>5.6 Amount of solder Excessive solder will induce higher tensile force in chip capacitor when temperature changes and it may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.</p> <hr/> <table border="0" data-bbox="513 940 1414 1354"> <tr> <td data-bbox="545 961 659 1031">Excessive solder</td> <td data-bbox="711 947 1089 1045">  </td> <td data-bbox="1114 947 1406 1045">Higher tensile force on the chip capacitor may cause cracking.</td> </tr> <tr> <td data-bbox="545 1108 659 1178">Adequate solder</td> <td data-bbox="711 1087 1203 1186">  </td> <td></td> </tr> <tr> <td data-bbox="545 1255 659 1325">Insufficient solder</td> <td data-bbox="711 1241 1089 1339">  </td> <td data-bbox="1114 1234 1406 1346">Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.</td> </tr> </table> <hr/> <p>5.7 Solder repair by solder iron</p> <p>1. Selection of the soldering iron tip Tip temperatures of solder iron varies by its type, P.C. board material and solder land size. Higher temperatures may provide quicker operation, however heat shock may cause a crack in the chip capacitor. Please confirm the tip temperature before soldering and keep the peak temperature and time in accordance with following recommended condition. (Please preheat the chip capacitors with the condition in 5.4 to avoid the thermal shock.)</p> <table border="1" data-bbox="578 1709 1406 1843"> <thead> <tr> <th colspan="4">Recommended solder iron condition (Pb-Sn Solder and Lead Free Solder)</th> </tr> <tr> <th>Temp. (°C)</th> <th>Duration (sec.)</th> <th>Wattage (W)</th> <th>Shape (mm)</th> </tr> </thead> <tbody> <tr> <td>300 max.</td> <td>3 max.</td> <td>20 max.</td> <td>Ø 3.0 max.</td> </tr> </tbody> </table>	Soldering	Temp. (°C)	Reflow soldering	$\Delta T \leq 150$	Manual soldering	$\Delta T \leq 150$	Excessive solder		Higher tensile force on the chip capacitor may cause cracking.	Adequate solder			Insufficient solder		Small solder fillet may cause contact failure or not hold the chip capacitor to the P.C. board.	Recommended solder iron condition (Pb-Sn Solder and Lead Free Solder)				Temp. (°C)	Duration (sec.)	Wattage (W)	Shape (mm)	300 max.	3 max.	20 max.	Ø 3.0 max.
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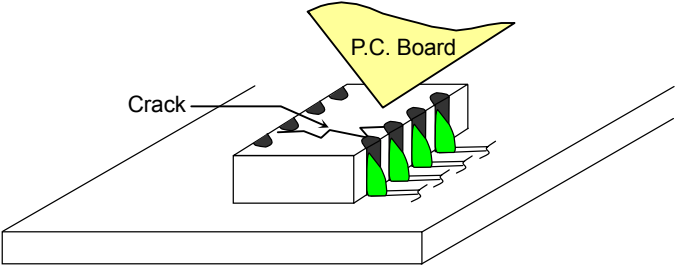
(10. Caution, continued)

No.	Process	Condition
5	Soldering (continued)	<p>2. Direct contact of the soldering iron with ceramic dielectric of the chip capacitor may cause cracking. Do not touch the ceramic dielectric and the terminations by solder iron.</p> <p>5.8 Sn-Zn solder Sn-Zn solder affects product reliability. Please contact TDK in advance when utilize Sn-Zn solder.</p> <p>5.9 Countermeasure for tombstone The misalignment between the mounted positions of the capacitors and the land patterns should be minimized. The tombstone phenomenon may occur especially when the capacitors are mounted (in longitudinal direction) in the same direction of the reflow soldering. (Refer to JEITA RCR-2335B Annex A "Recommendations to prevent the tombstone phenomenon")</p>
6	Cleaning	<p>1. If an unsuitable cleaning fluid is used, flux residue or some foreign articles may stick to the chip capacitor surface and deteriorate the insulation resistance.</p> <p>2. If cleaning condition is not suitable, it may deteriorate the chip capacitor's insulation resistance.</p> <p>2.1 Insufficient washing</p> <p>1. Lead wire and terminal electrodes may be corroded by Halogen in the flux.</p> <p>2. Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance.</p> <p>3. Water soluble flux has higher tendency to have above mentioned problems (1) and (2).</p> <p>2.2 Excessive washing</p> <p>1. Excessive washing may damage the coating material of coated capacitor and deteriorate it.</p> <p>2. When ultrasonic cleaning is used, excessively high energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, the following is recommended.</p> <p style="text-align: center;">Power: 20W/tmax. Frequency: 40kHz max. Washing time: 5 minutes max.</p> <p>2.3 If the cleaning fluid is contaminated, of Halogen concentration can increases, and bring the same result as insufficient cleaning.</p>
7	Coating and molding of the P.C. Board	<p>1. When the P.C. board is coated, please verify the impact on the capacitor.</p> <p>2. Please carefully verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor.</p> <p>3. Please verify the curing temperature.</p>

(10. Caution, continued)

No.	Process	Condition						
8	Handling after chip mounted	<p>1. Please pay attention not to bend or distort the P.C. board after soldering, otherwise the chip capacitor may crack.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Bend</p>  </div> <div style="text-align: center;"> <p>Twist</p>  </div> </div> <p>2. When functional check of the P.C. board is performed, higher pin pressure tends to be used for fear of loose contact. But if the pressure is excessive and bends the P.C. board, it may crack the chip capacitor or peel the termination. Please adjust the pins accordingly to ensure the P.C. Board is not flexed.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th data-bbox="506 798 652 850">Item</th> <th data-bbox="652 798 1044 850">Not recommended</th> <th data-bbox="1044 798 1435 850">Recommended</th> </tr> </thead> <tbody> <tr> <td data-bbox="506 850 652 1171">Board bending</td> <td data-bbox="652 850 1044 1171">  </td> <td data-bbox="1044 850 1435 1171">  </td> </tr> </tbody> </table>	Item	Not recommended	Recommended	Board bending		
Item	Not recommended	Recommended						
Board bending								
9	Handling of loose chip capacitor	<p>1. The chip capacitor may crack if dropped, especially large case sizes. Please handle with care and do not use if dropped.</p> <div style="text-align: center;">  </div>						

(10. Caution, continued)

No.	Process	Condition
9	Handling of loose chip capacitor (continued)	<p>2. When stacking the P.C. board for storage or handling after soldering, the corner of the P.C. Board may hit the chip capacitor of a neighboring board to cause a crack.</p>  <p>The diagram illustrates a 3D perspective of two printed circuit boards (PCBs) stacked on top of each other. The top board is labeled 'P.C. Board' and is shown in a yellowish color. The bottom board is white. On the bottom board, several electronic components are visible, including a chip capacitor. A line points to a crack on the top surface of this capacitor, labeled 'Crack'. The boards are shown being moved or stacked, with the top board's corner positioned over the capacitor on the bottom board.</p>
10	Capacitance aging	Class 2 capacitors have an aging characteristic, which is a decrease in capacitance over time due to crystalline changes that occur in ferroelectric ceramics. Careful consideration should be done in case of a time constant circuit.
11	Estimated life and estimated failure rate of capacitors	The estimated life and (failure rate) depend on the temperature and voltage. This can be calculated by the equation described in JEITA RCR-2335B Annex 6 "Calculation of the estimated lifetime and the failure rate." The risk can be decreased by reducing the temperature and the voltage but the failure rate can not be guaranteed.
12	Others	<p>The products listed on this specification sheet are intended for use in general electronic equipment (AV equipment, telecommunications equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment, industrial robots) under a normal operation and use condition.</p> <p>The products are not designed or warranted to meet the requirements of the applications listed below, whose performance and/or quality require a more stringent level of safety or reliability, or whose failure, malfunction or trouble could cause serious damage to society, person or property. Please understand that TDK is not responsible for any damage or liability caused by use of this product in any of the applications below or for any other use exceeding the range or conditions set forth in this specification sheet:</p> <p>Aerospace/Aviation equipment. Transportation equipment (cars, electric trains, ships, etc.) Medical equipment. Power-generation control equipment. Atomic energy-related equipment. Seabed equipment. Transportation control equipment. Public information-processing equipment. Military equipment. Electric heating apparatus, burning equipment. Disaster prevention/crime prevention equipment. Safety equipment. Other applications that are not considered general-purpose applications.</p> <p>When using this product in general-purpose applications, you are kindly requested to take into consideration securing protection circuit/equipment or providing backup circuits, etc., to ensure higher safety.</p>

11. Packaging label

Packaging shall be done to protect the components from the damage during transportation and storing, and a label which has the following information shall be attached.

- 1) Inspection No.
- 2) TDK P/N
- 3) Customer's P/N
- 4) Quantity

*Composition of Inspection No.

Example M 0 A - 00 - 000
 (a) (b) (c) (d) (e)

- a) Line code
- b) Last digit of the year
- c) Month and A for January and B for February and so on. (Skip I)
- d) Inspection Date of the month.
- e) Serial No. of the day

12. Bulk packaging quantity

Total number of components in a plastic bag for bulk packaging: 1,000pcs.

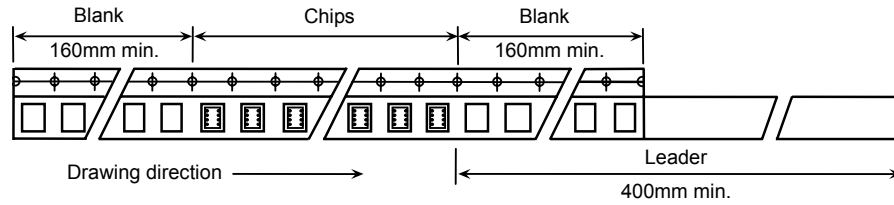
13. TAPE PACKAGING SPECIFICATION

1. CONSTRUCTION AND DIMENSION OF TAPING

1. Dimensions of carrier tape

Dimensions of plastic tape shall be according to Appendix 3.

2. Trailer and leader of carrier tape

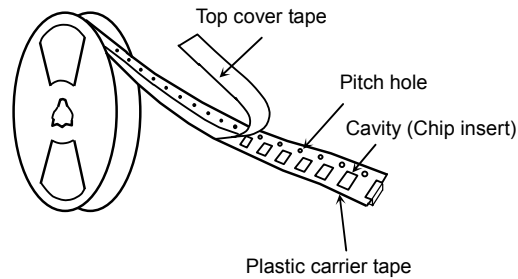


3. Dimensions of taping reel

Dimensions of 178mm diameter reel shall be according to Appendix 4.

Dimensions of 330mm diameter reel shall be according to Appendix 5.

4. Structure of taping



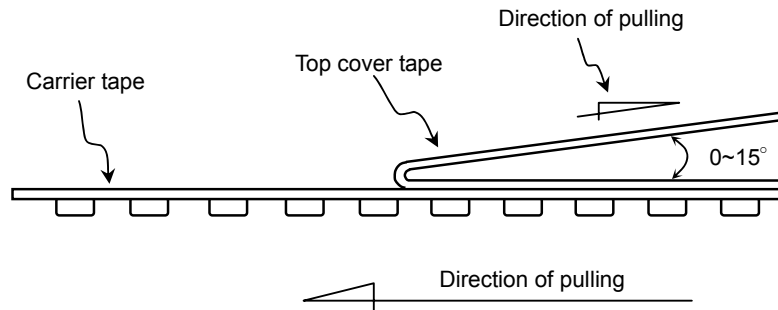
2. CHIP QUANTITY

Type	Taping Material	Chip quantity (pcs.)	
		Ø178mm reel	Ø330mm reel
CLLC1A [CC0603]	Plastic	4,000	10,000
CLLE1A [CC0805]	Plastic	4,000	10,000

3. PERFORMANCE SPECIFICATIONS

1. Peel back cover (top cover tape)

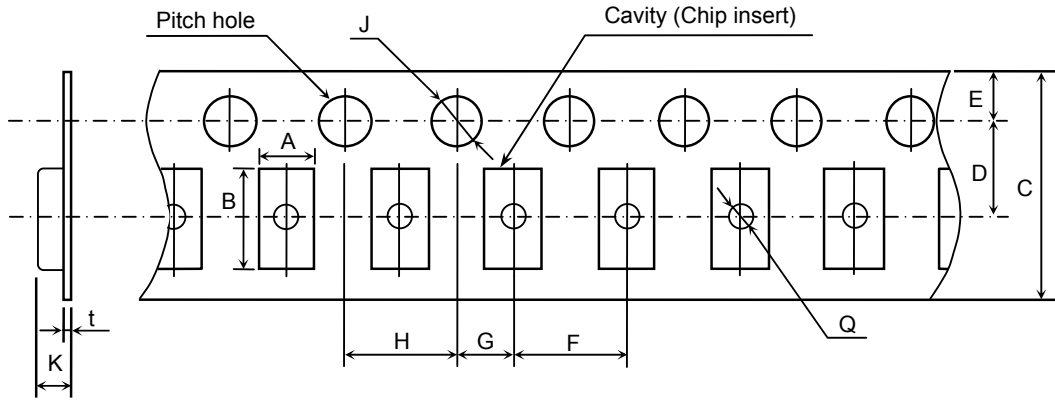
0.05-0.7N. (See the following figure.)



2. Carrier tape shall be flexible enough to be wound around a minimum radius of 30mm with components in tape.
3. The number of components missing shall be less than 0.1%
4. Components shall not stick to top cover tape.
5. The top cover tape shall not protrude beyond the edges of the carrier tape not shall cover the sprocket holes.

Appendix 3

Plastic tape



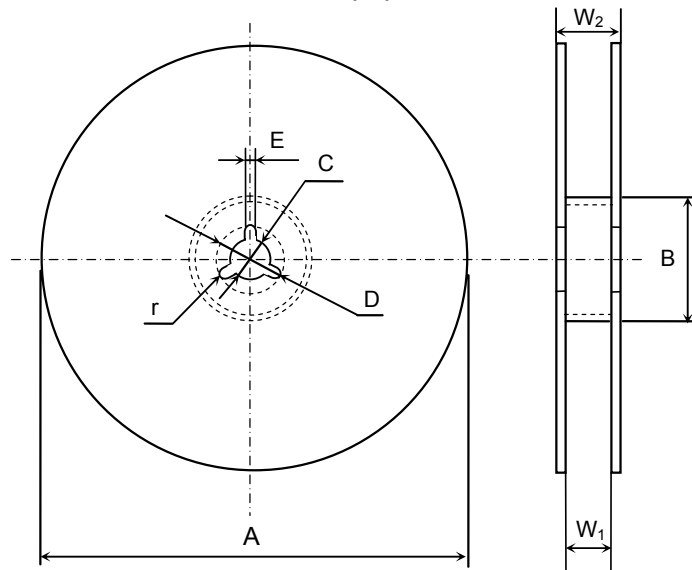
(Unit: mm)

Symbol Type	A	B	C	D	E	F
CLLC1A	1.1 ± 0.2	1.9 ± 0.2	8.0 ± 0.3	3.5 ± 0.05	1.75 ± 0.1	4.0 ± 0.1
CLLE1A	1.5 ± 0.2	2.3 ± 0.2				

Symbol Type	G	H	J	K	t	Q
CLLC1A	2.0 ± 0.05	4.0 ± 0.1	$\varnothing 1.5 \begin{smallmatrix} +0.1 \\ 0 \end{smallmatrix}$	2.5 max.	0.3 max.	$\varnothing 0.5$ min.
CLLE1A						

Appendix 4

Reel material: Polystyrene

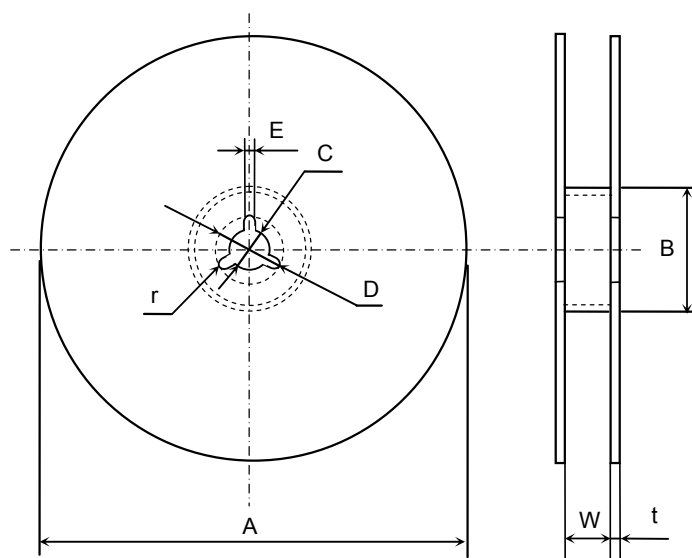


(Unit: mm)

Symbol	A	B	C	D	E	W1
Dimension	$\text{Ø}178 \pm 2.0$	$\text{Ø}60 \pm 2.0$	$\text{Ø}13 \pm 0.5$	$\text{Ø}21 \pm 0.8$	2.0 ± 0.5	9.0 ± 0.3
Symbol	W2	r				
Dimension	13.0 ± 1.4	1.0				

Appendix 5

Reel material: Polystyrene



(Unit: mm)

Symbol	A	B	C	D	E	W
Dimension	$\text{Ø}382 \text{ max.}$ (Nominal $\text{Ø}330$)	$\text{Ø}50 \text{ min.}$	$\text{Ø}13 \pm 0.5$	$\text{Ø}21 \pm 0.8$	2.0 ± 0.5	10.0 ± 1.5
Symbol	t	r				
Dimension	2.0 ± 0.5	1.0				

END PAGE